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LOW TEMPERATURE POLYSILICON THIN FILM TRANSISTORS IN ADVANCED DISPLAY TECHNOLOGIES

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FOR THE COMMANDER

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13. ABSTRACT *(Maximum 200 words)*

In this final project report, we detail the work completed in developing a polysilicon thin film transistor (TFT) technology that was successfully applied in fabricating a working VGA active matrix organic light emitting diode (AMOLED) display prototype. Using the high throughput, low cost method of rapid thermal processing (RTP), we achieved glass compatible crystallization temperatures of polysilicon. We identify that RTP results in superior TFT performance uniformity, which is critical for fabrication of AMOLEDs. We successfully developed and integrated novel microelectronic processes and techniques while fabricating AMOLED displays, culminating in the demonstration of a VGA AMOLED prototype display operated at a brightness of 101 nits. Using our high throughput, low cost process polysilicon TFT technology, we fabricated display driver circuits, including low temperature shift registers that run at clock frequencies as high as 20 MHz. Finally, several processing issues that were investigated in order to improve the performance of AMOLED displays are described. This includes work on low temperature silicides for TFTs, a novel hillock-free aluminum metallization, and the ability of this aluminum metallization to form ohmic contacts to indium tin oxide.

14. SUBJECT TERMS

Polysilicon Thin Film Transistors (TFT), low temperature crystallization, Rapid Thermal Processing (RTP), Active Matrix Organic Light Emitting Diode (AMOLED) displays, nickel silicide, cobalt silicide

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Goals of the Grant

The goal of this grant was to develop a polysilicon TFT technology compatible with low cost glass substrates for active matrix organic light emitting diode display (AMOLED) applications. To achieve this goal we focused on the following aspects:

- Develop a low temperature polysilicon crystallization process based on Rapid Thermal Processing as alternative to excimer laser, and investigate performance of polysilicon TFTs as a function of process conditions.
- Develop new polysilicon TFT and array metallization processes that include low temperature silicides, ohmic contacts to indium tin oxide, and hillock free aluminum.
- Design polysilicon TFT driver circuits and investigate their performance as a function of polysilicon microstructure.
- Design and fabricate a VGA active matrix array, demonstrating the first VGA AMOLED display.

Summary and Organization of Final Report

We had many successes throughout the work done under this grant. Some of these results were directly related to the goals of this project while others, though equally important to the success of the project, were solutions to problems that were not known at the beginning of this work. In this report we present our results into four chapters.

The first chapter describes our advances in polysilicon material. We set out to investigate a new crystallization technique, rapid thermal processing (RTP), to be used as alternative to excimer laser for crystallization of amorphous silicon. We achieved glass compatible crystallization temperatures using this high throughput and low cost process. We identify that RTP results in superior TFT performance uniformity, which is critical for fabrication of AMOLEDs.

The second chapter describes our work regarding the integration of polysilicon TFTs for active matrix organic light emitting diode displays. Several processes unique to AMOLED fabrication were developed. We successfully integrated all these processes and demonstrated a VGA AMOLED prototype display operated at a brightness of 101 nits.

The third chapter describes our successes in fabricating display driver circuits using our polysilicon TFT technology. We fabricated low temperature shift registers using a high throughput low cost process that run at clock frequencies as high as 20 MHz.

Finally, the fourth chapter describes in more detail some of the processing issues that were investigated to improve the performance of the AMOLED displays. Specifically the following processes are presented: a) low temperature silicides for TFTs, b) a hillock-free aluminum metallization, and c) ohmic contacts to indium tin oxide.

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Chapter 1

Development of Low Temperature Polysilicon Thin Film Transistors

The primary goal of this part of our work was to investigate the use of rapid thermal processing (RTP) for the crystallization of amorphous silicon films. In the process of conducting this research, other related topics were also covered such as the effect of polysilicon grain size on the carrier mobility.

1.1 Introduction

Active matrix liquid crystal displays (AMLCD) that utilize thin film transistors (TFTs) as the pixel-switching element currently dominate the field of flat panel. However, this technology is challenged by the new active matrix organic light emitting diode (AMOLED) display technology, which offers the following advantages: (a) improved viewing angle, (b) lower power consumption, and (c) potentially lower fabrication cost. At present, amorphous silicon is the dominant TFT technology however the new AMOLED displays will offer superior performance if the polysilicon TFT technology is used. Furthermore, the higher performance of polysilicon TFTs, compared to amorphous silicon TFTs, will enable the integration of display driver circuitry with the active matrix array on the same glass substrates. Integrating the driver circuitry onto the display panel can aid in reducing the cost of the display and improve its reliability. This has been a major driving force for developing a low temperature polysilicon TFT technology compatible with glass substrates by several manufacturers for AMLCD applications [1.1].

The deposition and crystallization of the polysilicon are two critical process steps that affect the polysilicon TFT performance, the display manufacturing throughput and the maximum process temperature. Since the polysilicon layer is first deposited in the amorphous phase, subsequent annealing must be done to crystallize the film. This anneal is one of the most thermally demanding fabrication steps. The polysilicon crystallization anneal has been traditionally accomplished with either furnace or laser annealing techniques. The furnace annealing process has a high thermal budget and a low throughput. For these reasons, excimer laser annealing (ELA) is currently the preferred annealing method [1.2]. However, the ELA process suffers from high cost, low throughput, and material uniformity problems. An alternative annealing technique, entitled RTP, has been recently introduced [1.3]. RTP uses two linear xenon arc lamps to rapidly heat and crystallize the silicon film as it is scanned underneath the lamps. RTP promises higher throughput than that of laser and furnace annealing as well as lower cost and better material uniformity when compared to laser crystallization.

However, the RTP crystallization process is still at its infancy and a lot of work is needed to demonstrate the potential of this new process for producing polysilicon films that meet the industries requirements of glass compatibility and TFT performance. Films with low crystallization temperatures ($<700^{o}$ C) are required for glass substrate compatibility while films with large grain size and small intra-grain defect density are required for high performance TFTs.

The goal of this work was to investigate the effect of various amorphous silicon deposition and RTP annealing process conditions on the amorphous silicon crystallization temperature, the resulting polysilicon micro-structure, and the performance of RTP processed polysilicon TFTs. The ultimate objective was the realization of high performance TFTs. In this work, statistically based experiments have been used to determine these effects. Both low pressure chemical vapor deposition (LPCVD) and plasma enhanced chemical vapor deposition (PECVD) processes were investigated for the deposition of the amorphous silicon. These are the most common deposition methods for amorphous silicon. PECVD deposition techniques are more commonly in industry for the deposition of amorphous silicon, but LPCVD deposition of amorphous silicon has been shown to produce larger grain polysilicon using the furnace annealing technique [1.4]. For these reasons both deposition methods were investigated.

For each set of deposition and annealing conditions, the polysilicon grain size, crystallization temperature, and TFT performance were measured. This allows the TFT performance to be correlated to the polysilicon microstructure (grain size) and the crystallization temperature. First, this chapter details the statistical experiments that were conducted to optimize the polysilicon films. Then, the results of the experiments are presented followed by a discussion of how the most important factors effect the crystallization temperature and the device performance.

1.2 Experimental

In order to meet the goals of this work, a series of statistically designed experiments were designed and conducted. Statistical models were then derived from the experimental results that quantitatively define the effects of the most important process parameters on the polysilicon crystallization temperature and device performance. These models are then used to understand how to co-optimize both the RTP crystallization temperature and the device performance.

A statistical approach was necessary to investigate a large number of variables with a manageable number of experiments. Also, a statistically based approach can investigate not only the effect of a set of variables on an experimental response, but also the effect of the interactions within the set of variables on an experimental response [1.5,1.6]. If each variable were optimized independent of the others, then these interactions would be ignored. This may lead to false conclusions since it is possible that some of the deposition and annealing variables may interact with each other.

The research was conducted in three experimental phases with each phase corresponding to a different method for the deposition of the amorphous silicon. The first phase investigated the RTP crystallization of amorphous silicon deposited by LPCVD using silane as the source gas. The second phase investigated amorphous silicon deposited by LPCVD using disilane as the source gas. The third phase investigated the deposition of amorphous silicon by PECVD. For each phase, "screening" experiments were conducted to determine and compare the linear effects of a variety of deposition and annealing conditions. A screening experiment is designed to investigate the linear response of a set of variables with the fewest possible runs. A run is defined as a unique set of process conditions. Each screening experiment consisted of either 8 or 16 different runs and investigated between 5 and 10 process variables. For the first screening experiment (LPCVD - silane source gas) two wafers were processed for each run. This

enabled the wafer-to-wafer reproducibility to be determined. For the rest of the experiments, one wafer was processed for each run and the reproducibility was assumed to be similar to that of the first screening experiment. For the PECVD experimental phase, a "response surface" experiment was also conducted after the screening experiment was complete. The goal of the response surface experiment was to investigate fewer parameters (4) in more detail. A response surface experiment can determine parabolic effects in addition to linear effects. The screening experiments can only determine linear effects.

Two eight-run screening experiments were designed to determine the importance of LPCVD deposition and RTP annealing conditions to optimize device performance and crystallization temperature. One experiment was conducted using silane as the source gas and the other was conducted using disilane as the source gas. The experimental set-up for both experiments is shown in Table 1.1. The columns represent the various deposition and annealing parameters to be investigated and the rows represent the individual experimental runs. Each run has a unique set of process conditions determined by the values indicated in the variable columns. If the value is a (+1), then the high value for that parameter is chosen, if the value is (-1) then the low value is chosen. The values for (+, high) and (-, low) are defined in the rows above the variable name. The three top rows of Table 1.1 represent the interactions between the various columns. For example, the "de" interaction indicates an interaction between Column D (film thickness) and Column E (RTP scan speed). A more detailed explanation of this experimental approach is found in reference [1.5].

In order to investigate amorphous silicon deposited using PECVD, a third screening experiment was designed. Due to the complicated nature of the PECVD deposition process, many more variables needed to be investigated. To accommodate the increased number of variables, a 16-run screening experiment was designed. The experimental set-up for the PECVD deposited material is shown in Table 1.2. After completion of the 16-run screening experiment, the four most important parameters were chosen for more detailed investigation. A response surface experiment was conducted using 27 runs and investigating three different levels for each variable [1.7]. Table 1.3 shows the response surface experimental set-up.

		de-	df-	ab-	ae-	ad-	ag-	af-
		fg-	eg-	dg-	bf-	bg-	bd-	be-
		cb-	ac-	ef-	cg-	cf-	ce-	cd-
	run #	A	B	C	D	E	F	G
silane	+	200 mT	580 C		100 nm	15 mm/s	LTO	Yes
experiment	-	100 mT	550 C		500 nm	5 mm/s	PECVD	No
		deposition pressure	deposition temp	dummy	film thickness	RTP speed	oxide type	preclean
disilane	+	160 mT	500 C		100 nm	15 mm/s	5 nm	
experiment	-	80 mT	470 C		50 nm	5 mm/s	0	
		deposition pressure	deposition temp	dummy	film thickness	RTP speed	seed thickness	dummy
	1	-1	-1	-1	-1	-1	-1	-1
	2	-1	-1	-1	1	1	1	1
	3	-1	1	1	1	1	-1	-1
	4	-1	1	1	-1	-1	1	1
	5	1	1	-1	-1	1	1	-1
	6	1	1	-1	1	-1	-1	1
	7	1	-1	1	1	-1	1	-1
	8	1	-1	1	-1	1	-1	1

Table 1.1 LPCVD screening experimental set-up. The investigated input parameters for the experiments using silane as the source gas and disilane as the source gas as shown.

					AD										
					BG	BD									
Alias	NO	HJ	IJ	HL	HM	HN	HO			BH	BI		BO	BL	
Structure	LM	LN	LO	IM	IL	IO	IN	BJ	DM	DN	DO	BM	DI	DJ	BM
	HI	MO	MN	JN	JO	JL	JM	DL	GN	GM	GL	DH	GJ	GI	GH
	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
+		1 T		300 W			350 C	disilane	Ar	1500 sccm		yes	yes	yes	15 mm/s
-		0.5 T		200 W			200 C	silane	H2	700 sccm		no	no	no	5 mm/s
		deposition		power			deposition	deposition	dilutant	dilutant		argon	RTP	hydrogen	RTP scan
		pressure					temp	gas	gas	flow		clean	dehydrog.	clean	speed
Run #															
1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
2	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1
3	-1	-1	-1	1	1	1	1	1	1	1	1	-1	-1	-1	-1
4	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1
5	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1
6	-1	1	1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1
7	-1	1	1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1
8	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1
9	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1
10	1	1	-1	-1	1	1	-1	1	-1	-1	1	1	-1	-1	1
11	1	1	-1	1	-1	-1	1	1	-1	-1	1	-1	1	1	-1
12	1	1	-1	1	-1	-1	1	-1	1	1	-1	1	-1	-1	1
13	1	-1	1	1	-1	1	-1	-1	1	-1	1	1	-1	1	-1
14	1	-1	1	1	-1	1	-1	1	-1	1	-1	-1	1	-1	1
15	1	-1	1	-1	1	-1	1	1	-1	1	-1	1	-1	1	-1
16	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1

Table 1.2 Experimental set-up for the PECVD screening experiment.

	Deposition Temperature (degrees C)	Deposition Pressure (Torr)	Deposition Power (Watts)	RTP Scan Speed (mm/s)
high value (+)	300	1.5	300	7
center value (0)	350	1	200	5
low value (-)	400	0.5	100	3

Table 1.3 Response Surface experimental set-up.

All amorphous silicon films were deposited on transparent four-inch quartz substrates. A 100 nm barrier oxide was deposited onto the quartz substrate followed by the amorphous silicon film deposition according to the conditions determined by the experimental set-up shown in Tables 1.1-1.3. The amorphous silicon film was then crystallized using RTP according to the experimental set-up. During the RTP process, the minimum process temperature required to crystallize the film was recorded. This temperature was measured using a pyrometer, which monitored the film as it emerged from underneath the lamps. The pyrometer was calibrated by passing a wafer with an embedded thermocouple through the RTP system. The error in measuring the crystallization temperature for a given run was less than 10° C and the variance for repeated depositions was 16° C.

In order to determine the effect of the deposition and annealing conditions on the device performance, TFTs were fabricated for all the experimental runs corresponding to a wide variety of polysilicon microstructures and crystallization temperatures. After crystallization, the polysilicon silicon islands were defined using wet etching. A 100 nm PECVD gate dielectric was then deposited followed by an amorphous silicon gate deposition. The gate electrode was then patterned and the islands and gate were doped

using a self-aligned process. Furnace annealing was then used to activate the dopants and to crystallize the amorphous silicon gate. The TFTs then received 300 nm of passivation oxide followed by contact holes and metallization. After the devices were completed they received an annealing treatment at 400° C in forming gas and one hour of plasma hydrogenation. A TFT crosssection is shown in Figure 1.1.

The devices were characterized in the linear region for four device parameters: the effective mobility, threshold voltage, sub-threshold slope, and the leakage current. Throughout the discussion in this chapter the emphasis will be placed on the carrier mobility. The other parameters are indicated in the tables. Unlike other device parameters, the carrier mobility is dependent mainly on the polysilicon microstructure. Other TFT parameters, such as the sub-threshold slope, threshold voltage, and leakage current, are all strong functions of the film thickness, [1.8] which varied up to 20% from its target value. For example, the thinnest LPCVD film (Run 1, LPCVD disilane experiment) had the greatest sub-threshold slope. The threshold voltage and sub-threshold slope are also strong functions of the quality of the gate dielectric and its interface with the polysilicon film. The leakage current can be very sensitive to charges in the dielectric underneath the channel. These charges can induce a back-channel and increase the leakage current. The mobility was chosen as the device parameter that measures the polysilicon material quality most independent of process variability and therefore is the best parameter in evaluating the quality of the different RTP crystallized polysilicon films.

The transistors were also characterized in the saturation region and the channel - length modulation parameter was extracted. This parameter is important because it determines the ability of a transistor to operate as a current source as well as determines the gain limitation of many polysilicon circuits, such as an inverter or operational amplifier.

The grain size of the polysilicon films was determined using transmission electron microscopy (TEM). The effective mobility was calculated from the maximum trans-conductance in the linear mode with V_{DS} = 1V for n-channel TFTs and V_{DS} = -1V for p-channel TFTs. The threshold voltage was determined as the voltage-intercept of the extrapolation of the linear part of the $I_D(V_{DS})$ characteristic. The sub-threshold slope was measured as the maximum slope of the [$\log(I_{DS})$ vs V_{GS}] plot. The leakage current was taken as the minimum drain current at V_{DS} = 5V for n-channel TFTs and V_{DS} = -5V for p-channel TFTs.

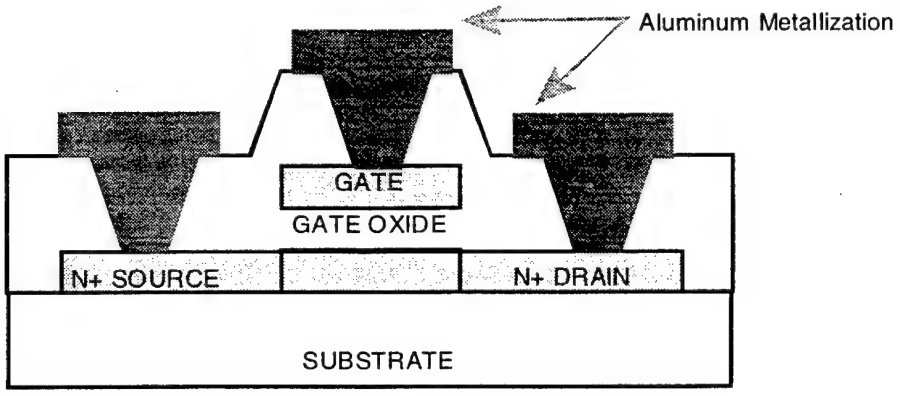


Figure 1.1 TFT Cross Section for n-channel TFTs.

1.3 Experimental Results and Statistical Models

The effect of the various deposition and annealing parameters on the TFT performance was analyzed using the statistical experimental structure. Each run resulted in TFTs with a set of experimental responses such as the average effective mobility or the crystallization temperature. The effect of any particular input parameter can be achieved by subtracting the average of all runs with a (+1) corresponding to that input variable with the average of all runs with a (-1) in that category. The resulting difference is referred to as the "effect". The larger the magnitude of the effect for a particular variable, the larger the impact that variable has on that experimental response.

Table 1.4 shows the output responses of the silane and disilane LPCVD screening experiments and Table 1.5 shows the calculated statistical Effects of each input variable for each experimental response. Tables 1.6 and 1.7 display the same information for the PECVD screening experiment. For the PECVD response surface experiment, TFT data was collected only for those runs (11 runs) achieving crystallization temperatures $<750^{\circ}$C. This data was enough to construct a model for the grain size, polysilicon crystallization temperature, and the TFT effective mobility as a function of the four input variables. These models are presented in Table 1.8. The coefficients that were insignificantly small were omitted.

	silane experiment					
run	Grain Size (nm)	C. T. (C)	N Mobility	Vth (V)	S	I leak
1	147	757	18.25	8.4	0.94	2.00E-12
2	152	788	26.9	10.1	0.64	5.00E-11
3	40	755	0.4	26.5	0.27	2.00E-09
4	44	729	1.1	23.5	0.51	5.00E-10
5	126	771	16.5	11.9	0.56	6.00E-09
6	152	759	27.2	7.1	0.58	2.00E-09
7	244	781	28.2	9	0.63	2.50E-10
8	195	779	23.6	7.6	0.61	6.00E-11

	disilane experiment					
run	Grain Size (nm)	C. T. (C)	N Mobility	Vth (V)	S	I leak (A)
1	367	730	27.8	5.7	1.21	5.00E-11
2	424	758	33.5	8.7	0.78	7.00E-11
3	358	771	35.7	7.3	0.775	4.50E-10
4	422	698	30.8	7.9	0.89	1.50E-10
5	296	751	15.7	11.9	0.71	1.00E-10
6	478	752	27.9	9.9	0.665	6.00E-10
7	711	700	36.5	8.35	0.705	7.00E-10
8	357	744	30	8.4	0.92	8.00E-11

Table 1.4 Output responses for the silane and disilane LPCVD screening experiments.

		A	B	C	D	E	F	G
silane	+	200 mT	580 C		100 nm	15 mm/s	LTO	Yes
experiment	-	100 mT	550 C		500 nm	5 mm/s	PECVD	No
		deposition pressure	deposition temp	dummy	film thickness	RTP speed	oxide type	preclean
Grain Size (nm)		8.4E+01	-9.4E+01	-1.4E+01	1.9E+01	-1.9E+01	8.0E+00	-3.5E+00
C. T. (C)		1.5E+01	-2.3E+01	-7.8E+00	1.2E+01	1.7E+01	4.8E+00	-2.3E+00
N Mobility		1.2E+01	-1.3E+01	-8.9E+00	5.8E+00	-1.8E+00	8.1E-01	3.9E+00
Vth (V)		-8.2E+00	8.5E+00	7.3E+00	3.3E-01	2.0E+00	1.2E+00	-1.9E+00
S		5.0E-03	-2.3E-01	-1.8E-01	-1.3E-01	-1.5E-01	-1.5E-02	-1.5E-02
I leak (A)		1.4E-09	2.5E-09	-1.3E-09	-5.7E-10	1.3E-09	6.8E-10	-1.4E-09
disilane	+	160 mT	500 C		100 nm	15 mm/s	5 nm	
experiment	-	80 mT	470 C		50 nm	5 mm/s	0	
		deposition pressure	deposition temp	dummy	film thickness	RTP speed	seed thickness	dummy
Grain Size (nm)		6.8E+01	-7.6E+01	7.1E+01	1.3E+02	-1.4E+02	7.3E+01	-1.3E+01
C. T. (C)		-2.5E+00	1.0E+01	-2.0E+01	1.5E+01	3.6E+01	-2.3E+01	0.0E+00
N Mobility		-4.4E+00	-4.4E+00	7.0E+00	7.3E+00	-2.0E+00	-1.2E+00	1.6E+00
Vth (V)		2.2E+00	1.5E+00	-1.1E+00	8.8E-02	1.1E+00	1.4E+00	4.1E-01
S		-1.6E-01	-1.4E-01	-1.9E-02	-2.0E-01	-7.1E-02	-1.2E-01	-3.6E-02
I leak (A)		1.9E-10	1.0E-10	1.4E-10	3.6E-10	-2.0E-10	-4.0E-11	-1.0E-10

Table 1.5 Statistical Effects for the silane and disilane screening experiments.

PECVD Screening Experiment						
Run #	Grain Size	C. T.	N Mobility	Vtn	S	I Leak
1	962	804	10.5	2.72	0.7	5.00E-10
2	1291	834	9.43	5.3	0.54	9.00E-10
3	783	829	8.93	7.44	0.466	1.60E-08
4	348	818	8.04	8.75	0.487	3.00E-10
5	1179	813	12.56	6.74	0.425	2.00E-10
6	718	846	7.14	8.72	0.444	1.50E-09
7	1031	804	8.81	8.97	0.594	5.00E-10
8	612	799	10.64	8.36	0.605	6.70E-08
9	1429	802	8.68	5.37	0.401	1.00E-09
10	1409	859	12.73	2.35	0.552	1.40E-10
11	1106	642	15.42	4.54	0.47	1.90E-08
12	773	813	7.18	8.5	0.628	4.00E-11
13	1361	851	9	7.72	0.461	2.00E-09
14	1171	841	14.5	3.16	0.302	3.80E-08
15	753	642	12.35	6.29	0.43	1.30E-09
16	707	822	12.06	5.2	0.639	1.00E-10

Table 1.6 Output responses for the PECVD screening experiment.

	A	B	C	D	E	F	G	H
+		**1 T**		**300 W**			**350 C**	**disilane**
-		**0.5 T**		**200 W**			**200 C**	**silane**
		deposition pressure		**power**			**deposition temp**	**deposition gas**
Grain Size	2.2E+02	1.1E+02	-7.1E+01	-9.4E+01	-1.2E+02	8.2E+01	-4.3E+02	1.1E+02
C. T.	-3.4E+01	-7.9E+00	2.1E+00	1.1E+01	5.4E+00	4.8E+01	-6.0E+01	-2.8E+01
N Mobility	2.0E+00	-2.0E-01	7.7E-01	-3.0E-01	-3.6E-01	-6.6E-01	-1.3E-01	1.3E+00
Vtn	-1.7E+00	8.7E-01	1.3E+00	1.4E+00	2.0E-01	5.1E-01	2.0E+00	-8.2E-01
S	-4.7E-02	1.2E-02	-4.3E-02	-9.7E-02	-5.7E-02	-5.1E-02	6.2E-02	-6.9E-02
I Leak	-3.2E-09	3.8E-09	9.1E-09	7.0E-10	-1.3E-08	1.3E-08	7.5E-09	7.8E-10
V Saturation	-1.3E+01	5.6E+00	-2.2E+00	1.7E+01	4.7E+00	-6.0E-01	1.8E+01	-9.7E+00

	I	J	K	L	M	N	O
+	**Ar**	**1500 sccm**		**yes**	**yes**	**yes**	**15 mm/s**
-	**H2**	**700 sccm**		**no**	**no**	**no**	**5 mm/s**
	dilutant gas	**dilutant flow**		**argon clean**	**RTP dehydrog.**	**hydrogen clean**	**RTP scan speed**
Grain Size	6.9E+01	4.4E+01	1.6E+02	8.2E+01	1.1E+02	-5.0E+01	-2.0E+02
C. T.	4.8E+01	-9.1E+00	9.9E+00	6.1E+00	-8.4E+00	-4.4E+01	5.6E+01
N Mobility	-3.2E+00	8.0E-02	1.7E+00	-9.7E-01	1.4E+00	-8.2E-01	-5.6E-01
Vtn	1.8E+00	2.7E-01	-6.0E-01	1.1E+00	-5.1E-01	1.2E+00	6.9E-02
S	2.5E-02	-6.9E-02	2.2E-02	1.1E-02	-5.4E-02	-5.9E-02	3.1E-02
I Leak	-1.3E-08	1.3E-08	7.8E-09	-1.7E-08	-3.6E-09	4.7E-09	8.4E-09
V Saturation	4.2E+00	2.3E-01	-1.9E+00	7.7E+00	-8.4E+00	4.7E+00	4.8E-01

Table 1.7 Statistical Effects for the PECVD screening experiment.

Coefficients	Crystallization Temperature	Grain Size	Mobility
Constant	346	1155	59
Temperature	-0.35	-2.2	-0.083
Power	-1.1	-0.71	-0.078
Pressure	290	900	-40
RTP Scan Speed	150	79	-0.63
RTP Scan Speed*Temperature	0.17		
RTP Scan Speed*Pressure	-40	-97	
[RTP Scan Speed]2	-11		
Temperature*Pressure			0.061

$$
\begin{aligned}
T_{cryst} = \; & 346 \\
& - 0.35 * \text{Temp} \\
& - 1.1 * \text{Power} \\
& + 290 * \text{Pressure} \\
& + 151 * [\text{RTP Scan}] \\
& + 0.17 * [\text{RTP Scan}] * \text{Power} \\
& - 40 * [\text{RTP Scan}] * \text{Pressure} \\
& - 11 * [\text{RTP Scan}]^2
\end{aligned}
$$

Table 1.8 Response surface models for TFT experimental outputs. Table shows the coefficients for the models for crystallization temperature, grain size and mobility. The actual formulation is shown below the table for the crystallization temperature.

From these tables, the variables critical to the optimization of TFTs for high performance and low crystallization temperature can be identified. The higher the relative value of the Effect, the more important that variable is. For example, for the LPCVD silane experiment, the most important factors in determining the grain size are the deposition pressure and the deposition temperature. This is deduced from Table 1.5 from the row labeled "grain size." In this row, the two variables having "Effects" that are much larger than the rest are the deposition pressure and the deposition temperature. Increasing the deposition pressure yields grain sizes that are on average 84 nm larger while decreasing the deposition temperature leads to grain sizes that are 94 nm larger.

1.4 Discussion of Experimental Results

Since there were 23 input variables investigated in the experiments, a large number of interesting observations and conclusions were made regarding the effect of these variables on the crystallization temperature, the polysilicon microstructure, and the resulting TFT performance. In the following part of this section our discussion focuses on the effects of three of the most important parameters; (a) the effect of deposition method, LPCVD or PECVD, (b) the effect of source gas, and (c) the effect of using a seed layer. In the next section we discuss the correlation between the polysilicon grain size and the TFT effective mobility.

1.4.1 Effect of Deposition Method - LPCVD or PECVD

The deposition method was determined to be important in determining device performance and crystallization temperature, but neither method could be concluded as universally superior. Each of these two deposition methods offers certain advantages over the other. The LPCVD-deposited amorphous silicon resulted in higher device performance, but the PECVD-deposited material resulted in lower crystallization temperature. Figure 1.2 plots the mobility as a function of the crystallization temperature for both the PECVD and LPCVD deposited polysilicon. The LPCVD devices had mobility up to 36 cm^2/V-s while the PECVD material resulted in a maximum mobility of only 15.4 cm^2/V-s. The lowest crystallization temperature in the LPCVD was 698° C while in the PECVD material was 595° C. It is worth noting that the PECVD experiments explored scan speeds bewteen 3 mm/s and 15 mm/s while the LPCVD experiments explored only between 5 mm/s and 15 mm/s. However, even at 5 mm/s, the PECVD experiments achieved crystallization temperatures as low as 642° C.

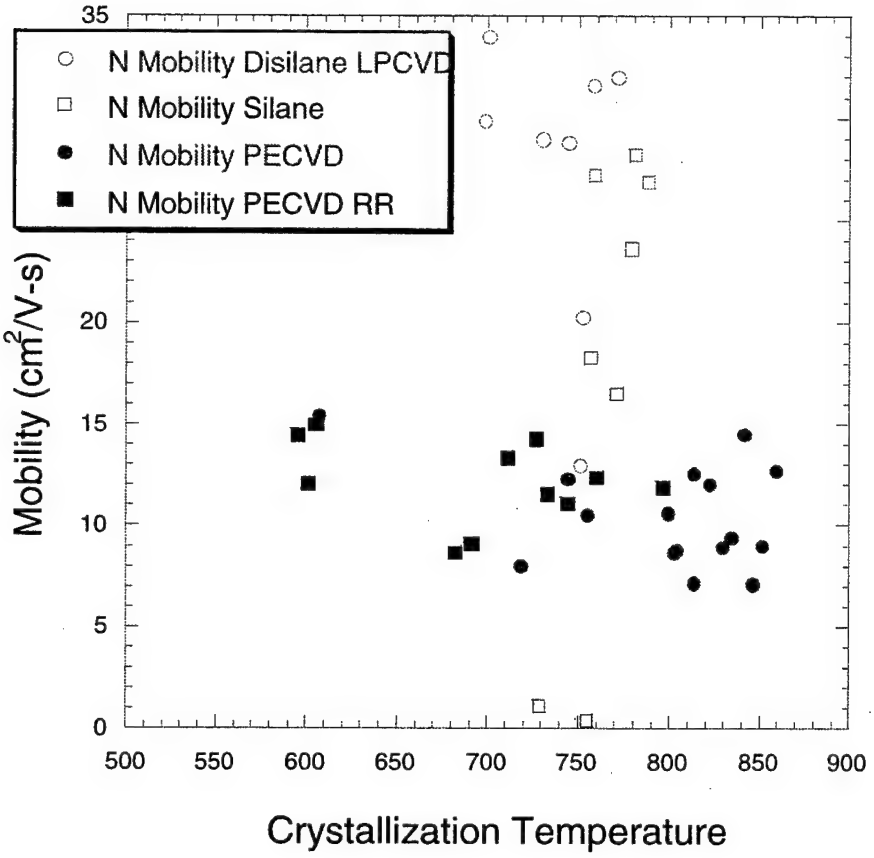


Figure 1.2 The mobility is plotted as a function of the crystallization temperature of the polysilicon material. A trend of higher mobility at lower crystallization temperatures can be seen, particularly for the LPCVD deposited material.

The LPCVD-deposited material produced higher performance TFTs and the PECVD deposited material produced lower crystallization temperatures. Figure 1.3 compares the I_{DS} - V_{GS} characteristics of the optimized LPCVD and PECVD materials. It can be seen that the TFT characteristics are similar but that the LPCVD characteristic has greater ON current due to its greater carrier mobility.

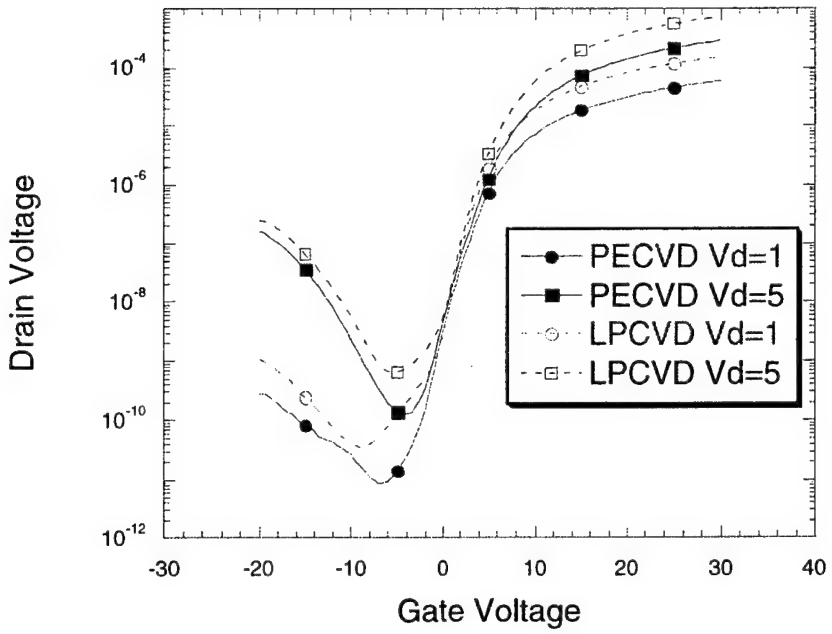


Figure 1.3 Comparison of LPCVD and PECVD deposited optimized TFTs. The LPCVD device has a mobility of 36 cm^2/V-s and a crystallization temperature of 700° C. The PECVD device has a mobility of 16 cm^2/V-s and crystallization temperature of 605° C.

1.4.2 Effect of Source Gas

The choice of source gas also had a major impact on TFT performance and crystallization temperature. Using disilane as the source gas produced polysilicon with lower crystallization temperatures and TFTs with better device performance compared with using silane as the source gas. This result agrees with previous work that used furnace annealing to crystallize the films [1.9]. Tables 1.4 and 1.6 indicate the lowest crystallization temperature and highest mobility were achieved using disilane as the source gas for both the PECVD and LPCVD experiments. This trend was particularly pronounced for the LPCVD experiments. For the disilane LPCVD experiment, the lowest crystallization temperature was 698° C and the highest average mobility was 36.5 cm^2/V-s. However, when silane was used, the lowest crystallization temperature was 729° C and the highest average mobility was 28 cm^2/V-s. Furthermore, the average crystallization temperature was lower for the disilane and the average mobility was higher for the disilane deposited films.

The benefit of using disilane as the LPCVD deposition source gas lie in its higher deposition rate at lower temperatures. Disilane is more reactive than silane and therefore decomposes at lower temperatures. At lower deposition temperatures, fewer crystallites will form resulting in fewer nucleation sites. Fewer nucleation sites result in larger grains and hence higher mobility. For silane, the required higher deposition temperatures result in

more ordered films with many crystallization sites already incorporated into the film which resulted in smaller grain size and hence lower mobility compared to disilane films.

1.4.3 Use of a Seed Layer for LPCVD Deposited Films

As mentioned above, larger grain size can be achieved by reducing the nucleation sites present in the film during deposition. However, this approach will tend to result in higher crystallization temperatures since the lack of nucleation sites will tender the film more difficult to crystallize. During the LPCVD disilane experiment, one of the variables investigated was the use of a seed layer. A seed layer is a very thin layer of amorphous silicon deposited prior to the actual film deposition. This seed film is optimized to have many crystallites and, as a result, have a low crystallization temperature. The thicker main film layer is engineered to have few crystallites and, on its own, a high crystallization temperature. However, when the two films are stacked together, the seed layer can induce crystallization of the film layer and result in a polysilicon layer that has a low crystallization temperature and a large grain size. Since larger grain sizes generally lead to improved polysilicon mobility, the use of a seed layer produces polysilicon films with high mobility and low crystallization temperature. Figure 1.4 plots the TFT mobility as a function of the crystallization temperature for only those films deposited by LPCVD. This plot is a subset of the information contained in Figure 1.2. It can be seen that without the use of a seed layer, lower crystallization temperatures lead to smaller grain size and lower mobility. However, the devices with a seed layer can have both a high mobility and a low crystallization temperature. The positive effect of the seed layer can also be deduced from the statistical model shown in Table 1.5. The seed layer reduces the crystallization temperature by an average of 23° C and increases the grain size by 73 nm.

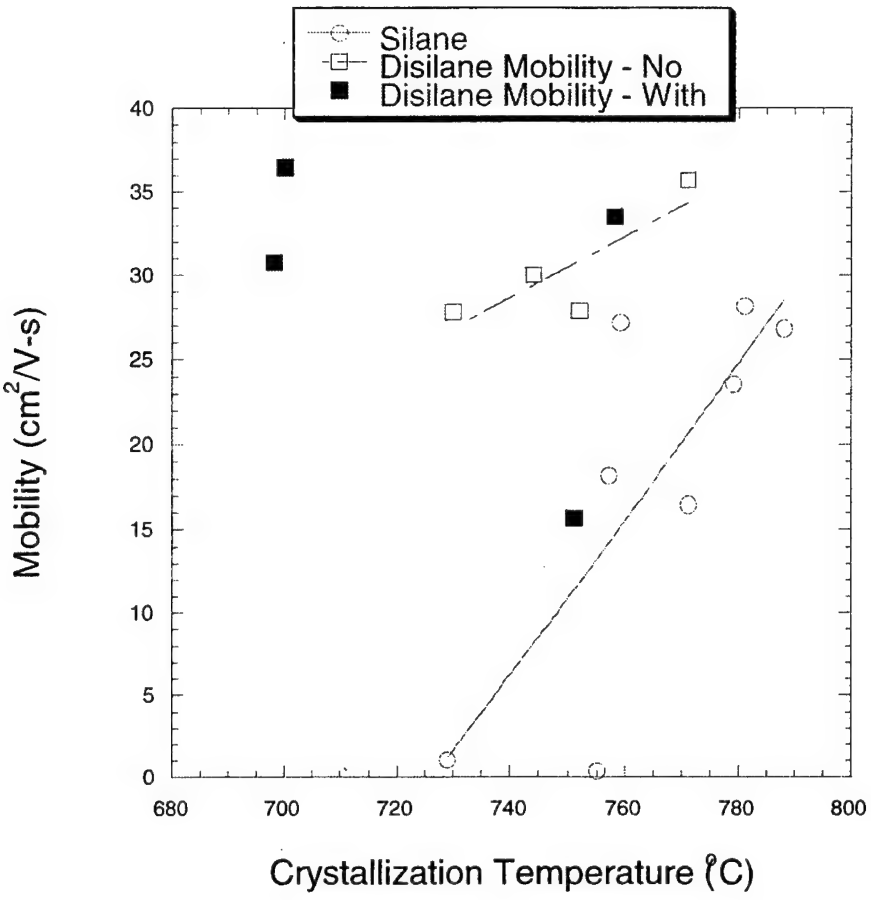


Figure 1.4 The mobility is plotted vs. the crystallization temperature for the LPCVD deposited TFTs. It can be seen that without the use of a seed layer, lower crystallization temperatures coincide with lower mobilities. However, when a seed layer is present, this trend can be avoided and high mobility was achieved at low crystallization temperatures.

When using the PECVD deposition method, the effect of the source gas is the same as for the LPCVD deposition method, but not as dramatic. The effect of the source gas can be determined by examining the experimental effects of the source gas column of the PECVD experiment in Table 1.7. Using disilane as the source gas increases grain size (11 nm) and increases mobility (1.3 cm^2/V-s) while reducing the crystallization temperature by an average of 28° C. This effect is significant but the 1.3 cm^2/V-s mobility improvement is not as large as the 12 cm^2/V-s average improvement obtained when using disilane LPCVD compared to silane LPCVD. This is not surprising since it is the plasma that dissociates the gases during the PECVD process as opposed to the thermal decomposition process that occurs during the LPCVD process. The thermal decomposition method should be more sensitive to the gas molecular structure.

1.5 Effect of Polysilicon Grain Size and Intra-grain Defects on Carrier Mobility

1.5.1 New Theoretical Model

In order to improve device performance by altering the deposition and annealing conditions of the polysilicon film, it is best to understand the mechanism for that improvement. One property of the film that theoretically impacts the device performance is the polysilicon grain size. Previous work has indicated that the mobility is a function of the polysilicon grain size. A formulation for the mobility as a function of the grain size is given in equation (1), where it is assumed that the grains are partially depleted and l_G represents the grain size and v_c is defined as $(kT/2\pi m_e)^{(1/2)}$ [1.10]. E_B is the barrier height caused by trapped carriers at the grain boundaries and is a function of the grain boundary defect density. An expression for E_B for a grain boundary in a polysilicon film is given in equation (2), where N_T represents the surface density of defects at a grain boundary (cm^{-2}), t_{ch} is the polysilicon channel thickness, and V_{TH} is the threshold voltage of the TFT [1.11]. Equation (1) indicates that an increase in grain size should lead to an increase in the carrier mobility.

$$\mu_{GB} = \frac{qv_c}{kT} l_G e^{\frac{-E_B}{kT}} \tag{1}$$

$$E_B = \frac{q^3 N_T^{\ 2} t_{ch}}{8\varepsilon_s C_{ox}(V_{GS} - V_{TH})} \tag{2}$$

Figure 1.5 plots the measured mobility as a function of the grain size for all of the deposition and annealing conditions considered in this work. It can be seen that, as a general trend, larger grain sizes lead to higher mobility as predicted by equation (1), but that the improvement of mobility with increasing grain size tends to saturate at large grain sizes. This saturation can be explained as being a result of intra-grain defects that exist in the polysilicon film. Due to the solid phase crystallization process that occurs during the RTP process, many defects within a grain may exist. The defects within a grain can trap charges and behave as coulombic scattering centers. When the contribution of the intra-grain defects is considered, the total mobility can be written according to equation (3) as a sum of the grain boundary limited mobility as well as the intra-grain mobility that is limited by coulombic scattering. An expression for the intra-grain mobility is given in equation (4) where N_I is the density of coulombic scattering centers [1.12].

$$\frac{1}{\mu_{Total}} = \frac{1}{\mu_{GB}} + \frac{1}{\mu_{IG}} \tag{3}$$

$$\mu_{IG} = \frac{113\varepsilon_s^{\ 2}(2kT)^{\frac{3}{2}}}{N_I q^3 m^{*\frac{1}{2}}} \left\{ \ln\left(1 + \left(\frac{12\pi\varepsilon_s kT}{q^2 N_I^{\frac{1}{3}}}\right)^2\right) \right\}^{-1} \tag{4}$$

From the data in Figure 1.5, the coefficient of grain boundary limited mobility can be extracted from the region of small grain size. Knowing this value, the intra-grain mobility

can be extracted by a using a best fit of equation (3) with the data. The intra-grain mobility for this solid phase crystallization process was extracted to be 58 cm^2/V-s. Using this value and using equation (4) and assuming that each defect in the film results in a Coulombic scattering center, the average level of intra-grain defects in these polysilicon films is extracted to be $3x10^{19}$ cm^{-3}.

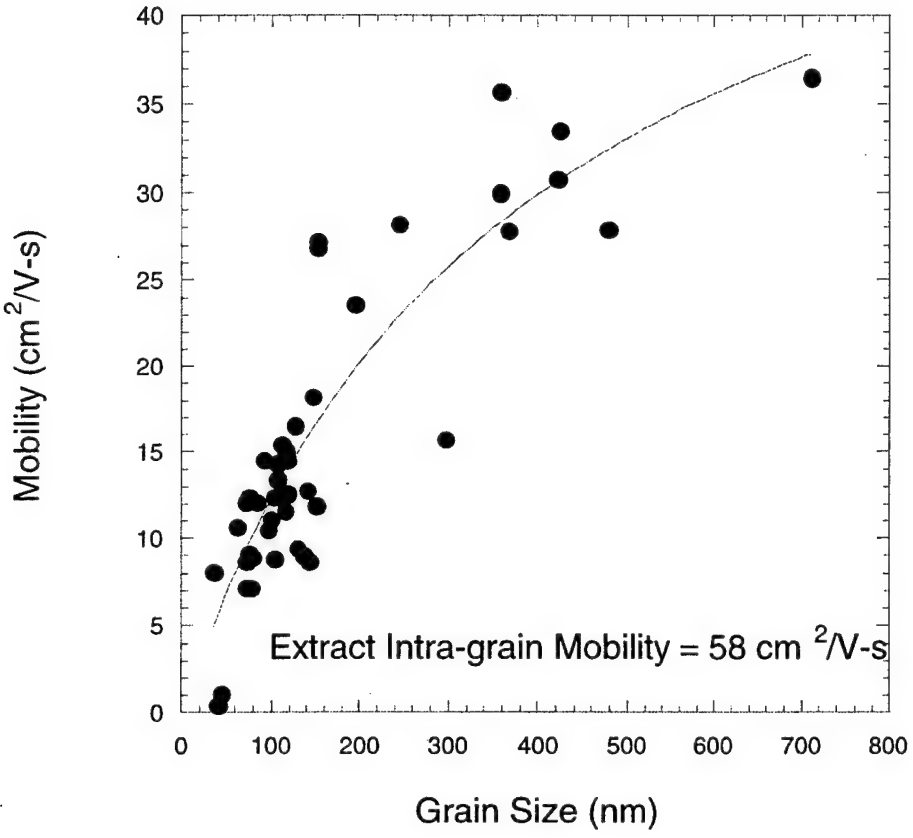


Figure 1.5 The mobility is plotted as a function of grain size.

The above approach has used the general trend observed in Figure 1.5 to extract the average density of intra-grain defects for all the polysilicon films considered in this experiment. However, there exists a large level of scatter in the data shown in Figure 1.5 compared to the model. One reason for this is because the level of intra-grain defects within the material may not be the same for all the polysilicon films. Although the grain size can be determined using TEM, it is much more difficult to determine a number for the level of intra-grain defects independent of the grain boundary defects.

Some of the deposition parameters that impact the level of intra-grain defects can be identified with the use of the statistical experimental design. If there were little scatter in

the data, the effects of the deposition and annealing parameters on the grain size should be the same as the effects on the mobility. Parameters that produce larger grains should produce higher mobilities. This was the case for all the variables investigated for the silane LPCVD experiment. Table 1.5 lists the effects of the various input parameters on TFT mobility. It can be seen that for the silane LPCVD experiment, the mobility is most impacted by the deposition pressure, deposition temperature, dummy column C (representing the interaction between the pressure and the temperature), and the film thickness. Furthermore, it can be seen that the parameters that affect the mobility also affect the grain size in a similar manner. Therefore, it can be expected that the grain size and mobility be closely related to each other for the silane deposited wafers. This is indeed the case as it is shown in Figure 1.6.

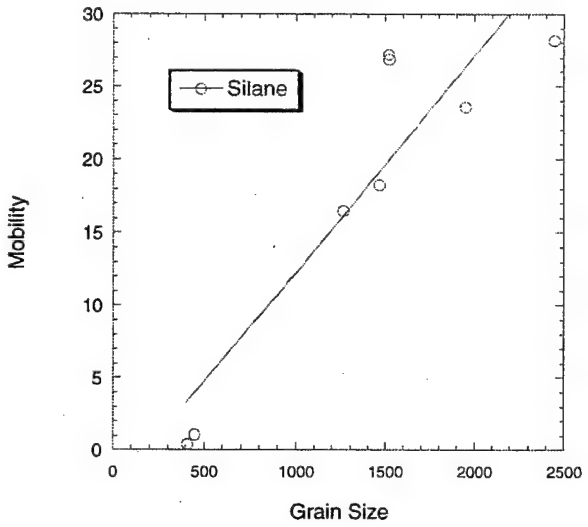


Figure 1.6 Mobility as a function of grain size for the silane LPCVD experiments. It can be seen that the mobility from the silane LPCVD runs correlate strongly with grain size.

However, unlike the silane LPCVD experiment, not all the variables investigated for the other experiments led to similar effects for the polysilicon grain size and the TFT mobility. Identifying a parameter that has different effects for the polysilicon grain size and the mobility can explain why the mobility does not depend strictly on the grain size. It is possible that such a parameter has a significant impact on the level of intra-grain defects in the polysilicon and therfore does not effect the TFT mobility and grain size in the same manner. The next section provides an example of two such variables.

1.5.2 Effect of Argon Dilution Gas and PECVD Deposition Temperature

From examining Table 1.7, it can be seen that the deposition temperature and the dilution gas both significantly impact the grain size. Lower deposition temperatures

produce larger grains (by 43 nm on average) and using argon as the dilution gas also leads to larger grains (by 7 nm on average). However, though lower deposition temperatures produce larger grains, they do not significantly increase the mobility as would be expected. Furthermore, using argon as a dilution gas also increases the grain size but significantly reduces the mobility, by 3.2 cm^2/V-s on average. Of the 16 runs, if the runs at lower deposition temperature or the runs that use argon as the dilution gas are omitted, the mobility correlates well with the grain size for the remaining runs. This trend can be seen in Figure 1.7, where the high deposition temperature, hydrogen dilution gas (instead of argon) runs are darkened and a best fit line with grain size is indicated.

As with the LPCVD experiments, a process variable that causes larger grain size without mobility improvements is likely causing an increase in the level of intra-grain defects. When argon is used as the dilution gas it is possible some of the argon is incorporated into the film. This argon incorporation would produce scattering centers (intra-grain defects) which reduce the carrier mobility independent of the polysilicon grain size.

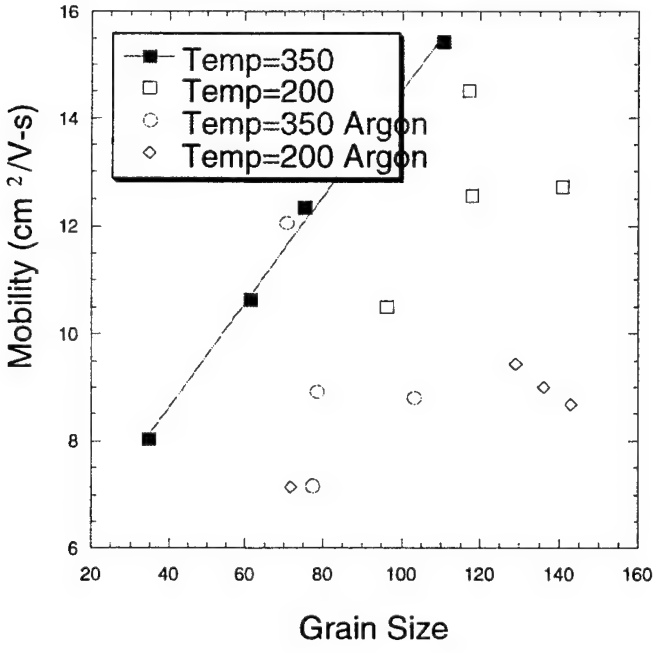


Figure 1.7 The mobility is plotted versus the grain size for the PECVD screening runs. In the case where the silicon was deposited at high temperature (350° C) and without argon as a dilution gas, the mobility correlates well with the grain size.

1.6 Conclusions

RTP is a viable alternative for the crystallization of polysilicon TFTs at glass compatible temperatures. The results of this study indicate that the crystallization temperature and TFT performance can be simultaneously optimized. A statistically based experimental design method was used to investigate the effect of a wide range of deposition and RTP annealing conditions on the TFT crystallization temperature and device performance. The importance of the deposition method (LPCVD vs. PECVD), deposition gas, and the use of a seed layer on the TFT performance and crystallization temperature have been discussed in detail. Other parameters important to device performance, such as dilution gas and deposition temperature have been identified. Polysilicon TFTs crystallized at temperatures as low as 600° C and thin film transistors with mobilities as high as 36 cm^2/V-s have been fabricated using the RTP crystallization process. A new theoretical model has been proposed that relates the carrier mobility to the grain size and intragrain defect density of the polysilicon film. This new model help us to explain some of the observed experimental results obtained in the case of PECVD films deposited using argon dilution. The new model can be used to extract the density of intragrain defects in the solid phase crystallized polysilicon films.

Chapter 2

Development of Polysilicon TFT AMOLED Displays

2.1 Introduction

A variety of technologies are currently in competition for a share of the flat panel display market. Currently, the dominant technology is the liquid crystal display (LCD), which operates by modulating light generated by a backlight. A new emissive technology, known as organic light emitting diode displays (OLED), recently has shown promise for high luminous efficiency (>10 lumens/watt), low voltage (<10V) and large viewing angle displays [2.1,2.2]. In these displays, current is passed through a thin multi-layer organic material where it is converted into light. One of the layers is an electron transporting material while the other is a hole transporting material. At the junction between the two is a layer optimized for luminous recombination where the carriers recombine and the excess energy is released as light. The wavelength of the light can vary depending on the dopant species used in this light-emitting layer [2.2,2.3]. The organic layers are sandwiched between a hole-injecting electrode consisting of a large work function material and an electron-injecting electrode consisting of a small work function material.

Since the most common electron injecting materials (Al-Li, MgAg) are opaque to visible light, the light must exit the structure through the hole injecting material. Therefore the hole injecting material must not only have a large work function, but must also be transparent to visible light. The most commonly used material is indium-tin-oxide (ITO) and this was chosen for this work.

Due to the nature of the light emission process, the brightness of the OLED material is proportional to the amount of current passing through it. Because of this, an active matrix pixel array needs to deliver uniform currents to the OLED material in order to create uniform light. This is different from AMLCD array technologies, which only need to deliver voltages, not currents, to switch the liquid crystal material. Therefore, different processing issues will arise for the development of AMOLED displays compared with AMLCD display technologies. This chapter discusses these issues and presents a fabrication process for AMOLED display arrays. First, the design strategy will be discussed and a justification for the need of polysilicon TFTs will be presented.

2.2 OLED Display Design Approach

OLED displays have been designed in both passive matrix and active matrix modes. In the passive matrix mode, each pixel consists of an overlap between two conductors, the address line, and the data line, with the OLED material in between. No transistors are required. To turn on a pixel, a certain voltage needs to be dropped across the OLED material. The address line delivers a fraction of this voltage, and the data line provides the remainder. A pixel receiving only part of the full voltage will be off. However, this approach limits the contrast and restricts the format of the display to smaller pixel counts. In addition, this approach requires patterning of both the hole-injecting and electron-injecting electrodes, which is difficult if MgAg is used as the electron-injecting electrode.

Using an active matrix design approach can solve the image contrast and MgAg electrode pattering problems. In the active matrix approach, a transistor is placed at each pixel to separate the effect of the data line voltage and the address line voltage on the voltage across the OLED material. A common MgAg electrode is used to eliminate the need to pattern the electron-injecting electrode. Within AMOLED designs, a variety of pixel architectures have been proposed [2.4]. Different pixel architectures may contain different numbers of transistors per pixel. The simplest design uses one transistor per pixel. A single transistor design approach has the advantage of increased contrast compared to a passive matrix design, and will have a higher yield than designs containing more than one TFT per pixel. However, in this approach each pixel is only pulsed ON for a fraction (1/(number of gate lines)) of the frame time. This requires the peak OLED current to be much higher than the average current, which leads to faster degradation of the OLED material.

To avoid the high current pulses native to the single TFT design, designs involving two transistors per pixel have been proposed which have pixel memory [2.4]. This memory allows the pixel to deliver a small current throughout the entire frame period. Though the average current through the OLED material is the same, the peak current is greatly reduced which leads to longer OLED material lifetime. Other architectures have also been proposed to improve brightness uniformity by correcting for variations in the transistor threshold voltage (≥ four transistors per pixel) [2.5]. Our work attempts to reduce brightness variations across the substrate through processing improvements rather than circuit design corrections. Both the one- and two-transistor-per-pixel designs are considered in this work. Figure 2.1 shows a schematic of these architectures.

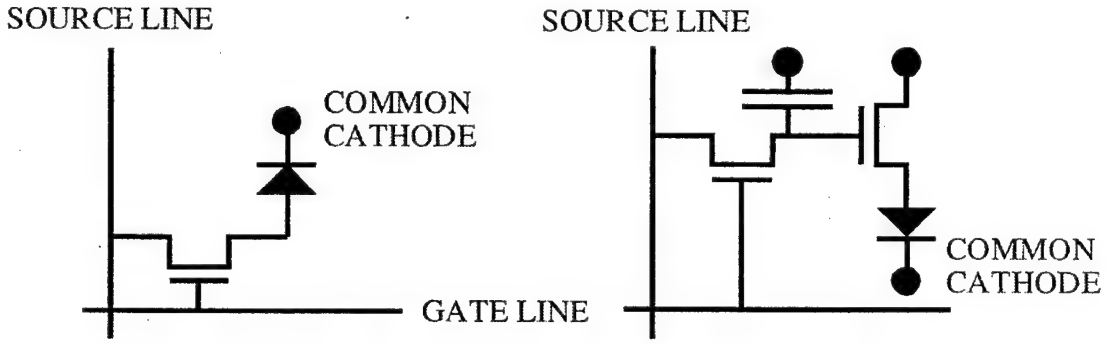


Figure 2.1 Pixel designs schematics showing (a) the single TFT per pixel design and (b) the two TFT per pixel design.

The next design issue is to determine which technology should be used to fabricate the transistor array. The most commonly used technologies for AMLCDs are amorphous silicon and polycrystalline-silicon (polysilicon). Both of these materials are compatible with large area glass substrate processes, which is necessary to fabricate displays at reasonable cost. Polysilicon TFT technology was chosen for its higher mobility compared with amorphous TFTs and its ability to provide p-channel devices. The higher mobility is

needed for the single TFT per pixel design because the pixels only emit light for a small fraction of the frame time and therefore large currents are required.

A calculation of the required mobility is as follows. The average current necessary to produce a bright display (100 cd/m^2) is approximately 10mA/cm^2 [2.6]. If we assume a pixel size of 50μm x 50μm, a steady current of 0.25μA is necessary. Since each pixel emits light only when it is activated by its address line, each address line is ON for only a small fraction (1/(# address lines)) of the frame time. Thus, in order to maintain an average DC current of 0.25μA, assuming 480 address lines, the maximum transistor current requirement (I_{MAX}) is 0.25μA x 480 = 240μA. Assuming a TFT operating in saturation, the required mobility can be calculated according to equation (1).

$$\mu = \frac{I_{\max}}{\frac{W}{2L} C_{ox} (V_{GS} - V_{TH})^2_{\max}} \tag{1}$$

Figure 2.2 shows a plot of transistor current in the saturation region as a function of gate voltage and mobility. For the above defined pixel area, adequate mobilities are those that yield currents greater than 240μA at a maximum gate voltage less than 10 V. To achieve the proper current levels using small device geometry (W/L = 2), and a gate oxide thickness of 50 nm, a mobility greater than 34 cm^2/V-s is required. Since a mobility of 34 cm^2/V-s is required, amorphous silicon cannot be used because it has mobilities less than 1 cm^2/V-s and therefore cannot deliver high enough currents with compact device geometry. Polysilicon-based transistors have mobilities more than an order of magnitude greater than amorphous silicon and therefore are a better candidate for AMOLED displays.

P-channel devices are desired to prevent variations in the OLED material turn on voltage from leading to current variations in the OLED material. To prevent these variations from affecting the light output, a current drive scheme is desired rather than a voltage drive scheme. To accomplish this, a p-type transistor operating in the saturation mode is used to drive current into the OLED material. When a p-channel transistor is used, both the gate and source voltages can be delivered directly to the transistor via the gate and data lines. If an n-channel TFT was used, only the gate voltage could be written directly to the pixel; the source voltage would depend upon the voltage across the OLED material. This assumes the direction of current flow is out of the transistor and into the OLED material, which is the case when the electron injecting material is not patterned. Therefore a p-channel transistor is the better candidate when a current drive scheme is desired rather than a voltage drive scheme. Since amorphous silicon technology cannot produce adequate p-channel TFTs; it is not a good candidate for AMOLEDs, even for the two-transistors-per-pixel designs where much smaller drive currents are required. Next, this chapter discusses the processing issues in matching polysilicon TFT technology with active matrix OLED displays.

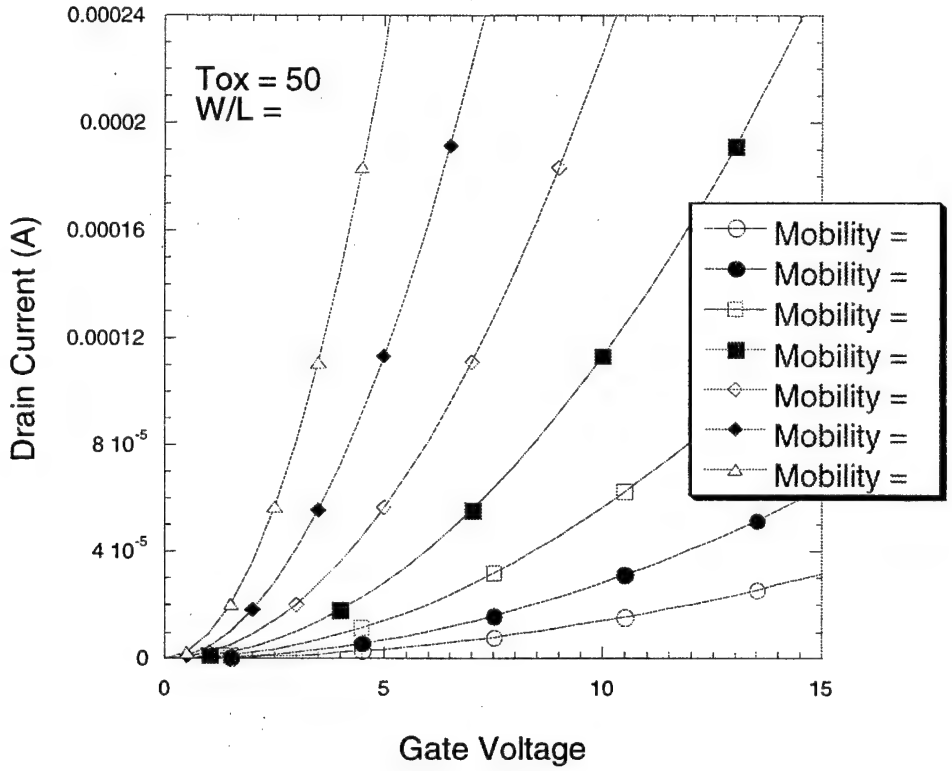


Figure 2.2 Mobility requirements for pixel transistors in AMOLED single TFT-per-pixel display designs.

2.3 AMOLED Polysilicon TFT Array Processing

This section describes a fabrication process used to realize both pixel designs. In both architectures (one transistor per pixel and two transistors per pixel), the current passes out of a transistor and into the OLED structure. Since the transistor controls the current through the OLED material, the uniformity of the transistor threshold voltage, carrier mobility, and series resistance is crucial to the final performance of the display array. This is because, to first order, the saturation TFT current can be written as shown in equation (2) where R_s represents a sum of both the series and contact resistance, μ_p represents the hole mobility, and V_{TH} represents the threshold voltage. To reach this equation (2) it has been assumed that the mobility degradation due to surface scattering is not significant.

$$I_{DS} = \frac{\frac{W}{2L}\mu_p C_{ox}(V_{GS} - V_{TH})^2}{1 + \frac{W}{L}\mu_p C_{ox} R_s (V_{GS} - V_{TH})} \quad (2)$$

It is evident from equation (2) that variations in the threshold voltage, carrier mobility, or series resistance will directly impact the uniformity of the TFT current and consequently, the brightness of the display. In this work, a variety of steps were implemented to reduce the series resistance and improve the uniformity of the pixel electrical characteristics. The carrier mobility and threshold voltage variations were reduced through the use of RTP for polysilicon crystallization to achieve uniform polysilicon microstructure. A silicidation process was developed to eliminate TFT series resistance and a low resistance contact scheme was developed to connect the ITO to the drain of the TFT. Finally, a planarization scheme based on spin on glasses (SOGs) was used in order to provide a smooth and uniform surface prior to OLED material deposition. These steps are described below along with a process used to fabricate the display arrays.

The fabrication process is divided into four parts: (a) silicon island preparation, (b) TFT silicidation, (c) ITO electrode and metallization, and (d) final array passivation. A cross section of the process indicating these four areas is shown in Figure 2.3.

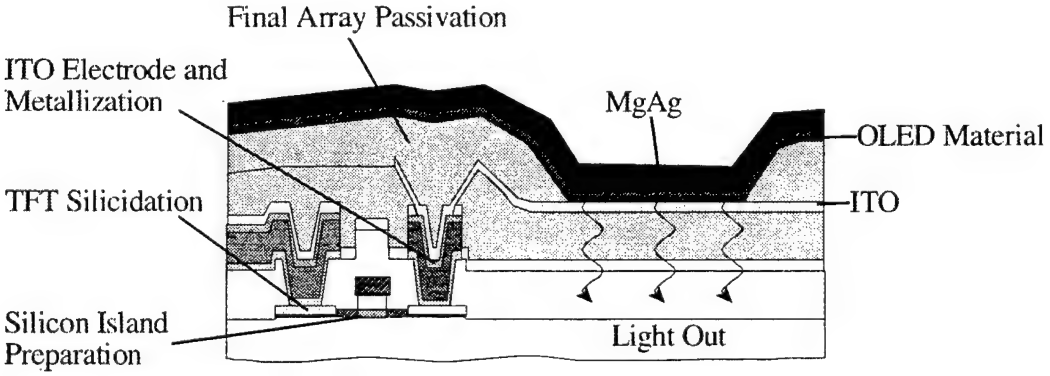


Figure 2.3 AMOLED array process overview.

2.3. Silicon Island Preparation

The silicon films were deposited by pyrolysis of disilane in a low pressure chemical vapor deposition reactor at a temperature of 470° C or 500° C. The films were then crystallized into the solid phase using RTP. The RTP process was chosen over alternative crystallization methods, such as ELA, because of its high uniformity and high throughput [2.7]. The uniformity of heating during crystallization is important to create uniform polysilicon microstructure across the wafer. In the ELA process, due to the narrow localization of the light beam and the melting of the silicon film, significant microstructure variations can result. In contrast, the wide profile of the RTP lamp and the solid phase crystallization nature of the process results in uniform polysilicon microstructure. The RTP throughput is determined by the speed with which the wafers are passed underneath the

heating lamps. For this work, scan speeds of 5mm/s or greater were used. The RTP crystallization temperatures were in the range of 677° C to 720° C. The thickness of the polysilicon islands was 50 nm.

After the amorphous silicon films were crystallized and patterned, a 100 nm gate oxide and a 100 nm amorphous silicon gate were then deposited by PECVD. The wafers were then annealed in a furnace to crystallize the amorphous silicon gate, though a second RTP step could have been used. The gate electrode was then patterned and the gate, source, and drain were doped either with phosphorus or boron to a dose of 2×10^{15} cm^{-2}. The dopants were activated at 800° C in a furnace, though again RTP could be used for dopant activation.

2.3.2 TFT Silicidation

Nickel silicides were formed on the source, drain, and gate regions to reduce the series resistance of the TFT. The gate region directly on top of the channel was not silicided because of the use of an oxide mask. This mask was necessary to preserve a p+ region in contact with the channel to maintain a blocking junction and thus proper device operation. The silicidation step becomes increasingly important as polysilicon islands are reduced in thickness, because thinner islands increase the series resistance of the TFT. It is desirable to reduce the polysilicon island thickness to improve the TFT performance and to increase manufacturing throughput. Our previous work has shown that the use of silicides can enable ultra-thin (<30 nm) island TFTs to be made without significant reduction in the ON current due to the island series resistance [2.8]. Furthermore, since the silicidation process reduces significantly the source and drain parasitic series resistance and its associated variability, the uniformity of the TFT is expected to improve.

The silicides were formed by sputter depositing Ni onto the wafers followed by an in-situ vacuum anneal at 400° C for 10 minutes. The silicided source and drain regions had a sheet resistance of 20 Ohms/square, whereas the non-silicided regions had a sheet resistance of 800 ohms/square. Since the polysilicon gate lines were also silicided, the gate line resistance was improved by a factor of 40 compared with a non-silicided polysilicon gate. Figure 2.4 (a) shows a pixel cross-section after the silicide stage in the array fabrication process.

It is important to note that NiSi is resistant to both reactive ion etching and wet etching of silicon dioxide [2.9], and thus it can be used as an effective etching stop for the opening of the source and drain contact windows. Doped silicon is not as resistant to dry etching as nickel silicide. This is another advantage of using the nickel silicided source and drain process.

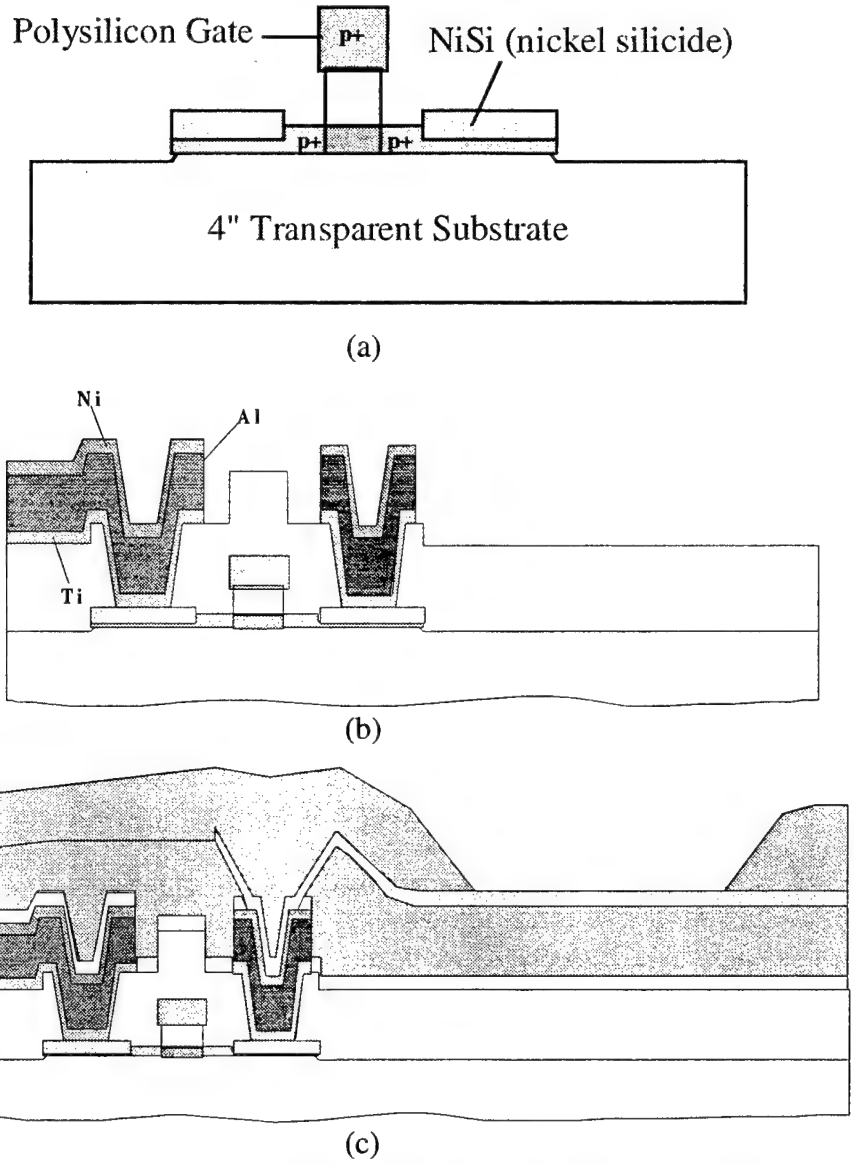


Figure 2.4 Cross sections of the array pixel at three different stages of processing: (a) after TFT formation, (b) after metallization, and (c) the final pixel cross-section.

2.3.3 ITO Electrode Formation and Metallization

After the transistor formation, 300 nm of PECVD passivation oxide was deposited to cover the islands and gates and to prevent shorts between gate and data lines. Contact holes were then opened to the gate and island regions using wet etching followed by deposition of the data metals. The data metallization consisted of a three-layer stack to prevent the formation of hillocks. The layers were 50 nm of Ti, 200 nm Al, and 50 nm of Ni. A cross section of the pixel at this stage is shown in Figure 2.4(b). It was found that the Ti alone could not prevent the formation of hillocks during hydrogenation, but that the addition of an extra layer of nickel on top of the aluminum prevented the formation of

hillocks [2.10]. Figure 2.5 compares atomic force microscope (AFM) images of an Al film with a Ni capping layer with an Al film with no capping layer after both films have been annealed at 500° C. It is clear that the nickel layer prevents the formation of hillocks even at temperatures far greater than those required for AMOLED processing. This is an important consideration in OLED displays because a hillock can cause a short between the data line and the common cathode of the OLED material. Figure 2.6 shows an example of OLED display damage that may occur from a hillock. After metallization, the wafers were plasma hydrogenated for one hour at 300° C.

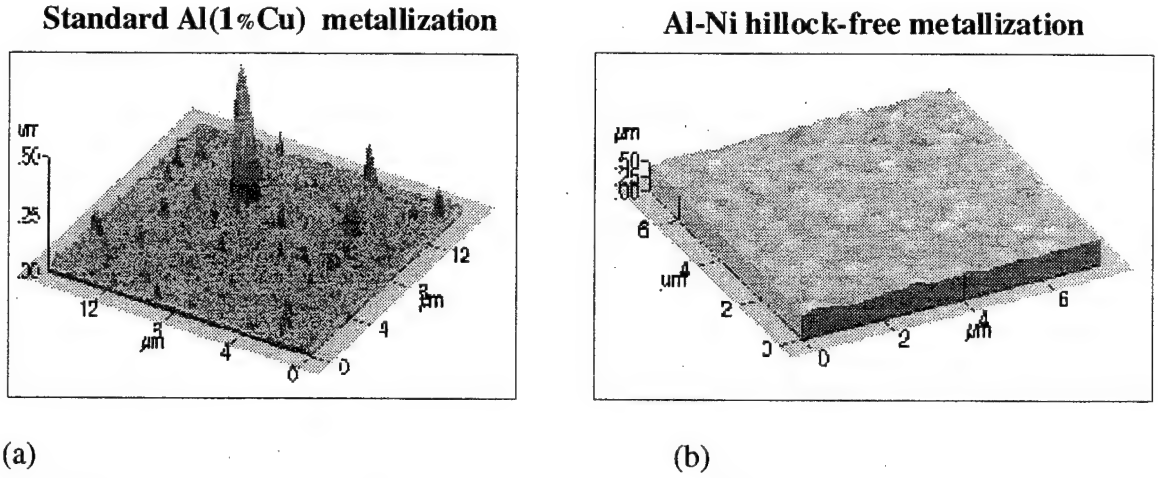


Figure 2.5 This figure compares AFM pictures of (a) an Al film and (b) an Al-Ni film after both films were heated at 500° C. It is clear that the Al-Ni film resists the formation of hillocks.

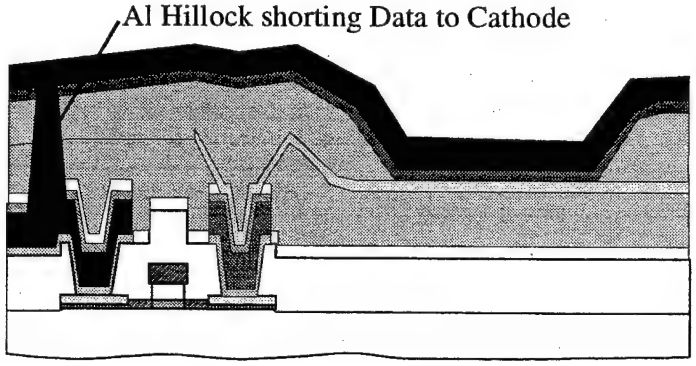


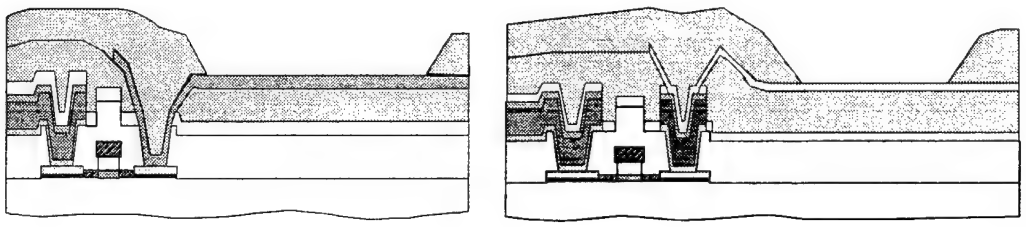
Figure 2.6 This figure shows how an Al hillock can short a data line to the common cathode of the AMOLED structure.

The data metals were then covered with a double layer of PECVD oxide and spin on glass (SOG). The SOG was cured on a hot plate at 300° C. A higher cure temperature was not used because it may have instigated out-diffusion of hydrogen and reduced the performance of the TFTs. The combination of these two dielectric provided excellent

protection of the metals from future corrosive etches as well as a smooth, well-planarized surface for the deposition of the ITO electrode. It is important that the ITO electrode resides on a well-planarized surface so that the surface of the ITO is free of any asperity that might cause non-uniform current flow across the OLED material. A contact hole was then opened in the SOG and oxide so that the ITO could connect to the drain of the TFT. The ITO was sputter deposited at 200° C.

Two different approaches were investigated to contact the ITO electrode to the silicided polysilicon island. In one approach, the ITO contacted the silicided island directly. In another approach, the ITO contacted a data metal plug, which in turn contacted the silicided island. Figure 2.7 shows a comparison of these two contact approaches. Both processes were used in order to investigate which process could provide more uniform pixel characteristics.

In the metal plug approach, the Ni capping layer in the Ti-Al-Ni stack is necessary not just to prevent hillock formation, but also to ensure a good contact of the ITO to the metals. Previous work has demonstrated that the Al-ITO forms an interfacial oxide and the contact is not ohmic. However, adding a Ni capping layer prevents the formation of this oxide and the Al-Ni-ITO forms a low resistance, ohmic contact [2.11].



(a) (b)

Figure 2.7 Two different processes are shown to contact the ITO to the silicided polysilicon island; (a) the ITO contacts the silicide directly, and (b) the ITO contacts a data metal plug which then contacts the silicide.

2.3.4 Final Array Passivation

After the ITO patterning, a second SOG dielectric was spun onto the wafer and cured on a hot plate at 275° C. This cure temperature was chosen to be less than the cure temperature of the previous SOG layer in order to prevent stressing and possibly cracking the previous SOG film. A contact hole was then patterned and etched using wet chemistry to open an area where the OLED material would contact the ITO. This window defines the area from which light will be emitted. The use of wet chemistry is important at this stage in order to provide a gradual slope in the etched passivation oxide around the OLED window formed on top of the ITO. A gradual slope is important in order to achieve good step coverage of the OLED material.

Also, in order to guarantee a smooth surface for the OLED material, this final cut to the ITO was placed only over the area of the ITO that has minimal topological variations underneath it. The SOG underneath the ITO will ensure that the ITO is smooth except

where this SOG has been etched for the ITO-data metal contact, while the SOG on top of the ITO will planarize the region where the ITO contacts the metal plug. Thus, a smooth topology is provided for the OLED material. A smooth surface prior to OLED material deposition will minimize unwanted OLED material thickness variations and therefore improve the brightness uniformity of the display. Figure 2.4(c) shows a final cross section of the pixel prior to OLED material deposition.

2.4 Array Performance

The four major process improvements discussed above were all important to the final array performance. The RTP process achieved uniform polysilicon characteristics. The silicidation and ITO contact step reduced parasitic series resistance and therefore further improved uniformity. The metallization was hillock free and prevented shorts to the OLED common cathode. Finally, the passivation and planarization produced a smooth ITO surface prior to OLED material deposition.

To determine the uniformity of polysilicon TFTs crystallized using the RTP process, data was collected from wafers processed by RTP. The local uniformity was determined by measuring the standard deviation of threshold voltage over the area of one die (0.25 cm^2). The global wafer uniformity was determined by evaluating the data over an area of 10 cm^2. The local variation was 65mV for n-channel TFTs and 140mV for p-channel TFTs. The global variation was 100mV for n-channel TFTs and 150mV for p-channel TFTs. This data confirms that the RTP crystallization process leads to highly uniform polysilicon TFTs.

The silicidation process also was found to improve the uniformity of the TFTs. Figure 2.8 shows a cumulative probability plot comparing TFTs fabricated with silicides to TFTs fabricated without silicides. For a large group of silicided or non-silicided devices, the value of V_{GS} was determined to achieve a median current level of 20 μA, at V_{DS} = 1V. Then, the individual devices were measured to determine the exact drain current of each TFT at this fixed V_{GS} value. The percent deviation from the median current (the target current) was then measured for each TFT. This graph plots the deviation in the targeted current as a function of the percentage of devices. This method takes into account both mobility and threshold voltage non-uniformity and therefore best imitates the non-uniformity in TFT pixel current. From Figure 2.8, it is clear that the silicided devices are more uniform. For example, 80% of the silicided devices have currents that vary within 2% of each other, whereas the non-silicided devices have currents with variation greater than 5%. This increase in uniformity is attributed to a reduction in the variable series resistance.

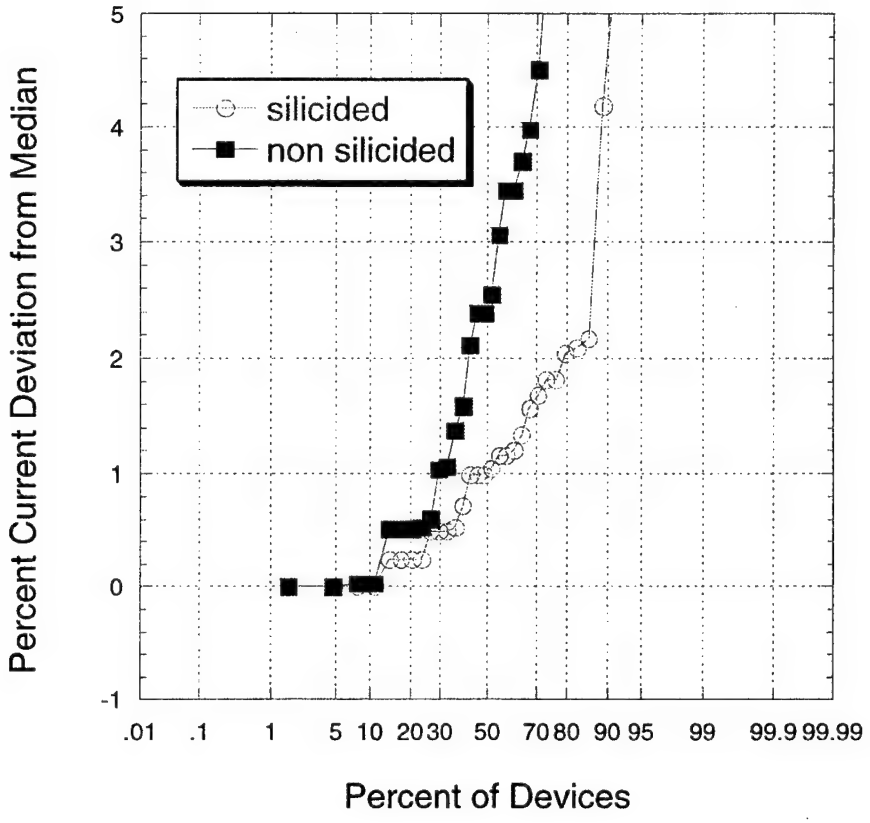


Figure 2.8 This figure shows a cumulative probability plot of TFT drain currents falling within a percentage of the median current. It can be seen that the silicided devices are more uniform.

In addition to TFT silicidation, it was also found that the method of contacting the ITO to the silicon island was critical in determining the parasitic resistance of the pixel. The series resistance resulting from connecting the ITO directly to the silicided island was intolerably high and significantly deteriorated the pixel drive current. This is because when the ITO was in direct contact with the nickel silicide an interfacial oxide was formed. This contact then was no longer ohmic in nature. However, when adding the metal plug between the ITO and the NiSi, the contact was ohmic and parasitic resistance had only a minor effect on the pixel performance. The contact resistance using the ITO-metal-silicide contact scheme was 480 $\mu\Omega$-cm^2 at a bias of 1 V. In contrast, the contact resistance of the ITO-silicide scheme was 33 mΩ-cm^2, even at a bias of 10V.

To illustrate the advantages of this new contact method, Figure 2.9 shows the linear transfer characteristics of the completed pixels using the ITO-metal-silicide contact method as well as the ITO-silicide contact method. A control TFT is also shown which has no ITO connection, but rather the silicide was probed directly. It can be seen that pixels using the

ITO-silicide contact suffered greatly due the contact resistance, but that the pixels using the ITO-metal-silicide contact does not have this problem and achieves characteristics similar to the control TFT.

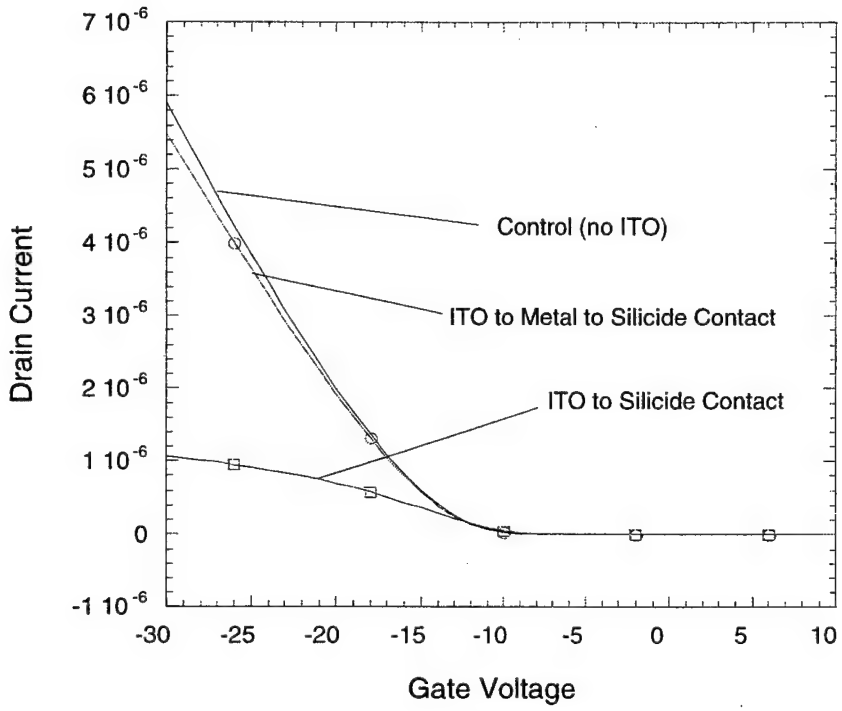


Figure 2.9 TFT transfer characteristics comparing a TFT using an ITO-metal-silicide contact scheme with a TFT using an ITO-silicide contact scheme.

VGA size arrays with a 4-cm diagonal were fabricated using the process described above. Figure 2.10 shows a photograph of a completed wafer prior to organic material deposition and Figure 2.11 shows a microscope photograph of a completed pixel having the single-TFT-per-pixel design. The pixel size is 50 μm by 50 μm. Figure 2.12 shows a transmission mode photograph of a pixel having the two-TFT-per-pixel design; its pixel size is 100 μm by 100 μm.

The pixel functionality was tested by probing the ITO pad and applying test voltages to the periphery of the array. Pixel TFT characteristics were measured for n-channel and p-channel wafers and for wafers with both types of ITO to island contacts. Figure 2.13 shows the transfer characteristics at V_{DS} = -1V of a p-channel TFT in the single TFT pixel structure. The p-channel pixel TFT has a mobility of 21 cm^2/V-s and the n-channel pixel TFT has a mobility of 46 cm^2/V-s. These characteristics were measured for the case where the ITO contacts the NiSi via a metal plug. After the completion of the arrays, the OLED material was deposited and the displays were tested. An average brightness of 101 cd/m^2 was obtained at a frame rate of 60 Hz [2.12]. The operating AMOLED display testifies to

the success of the active matrix array panel and the fabrication approach discussed in this section.

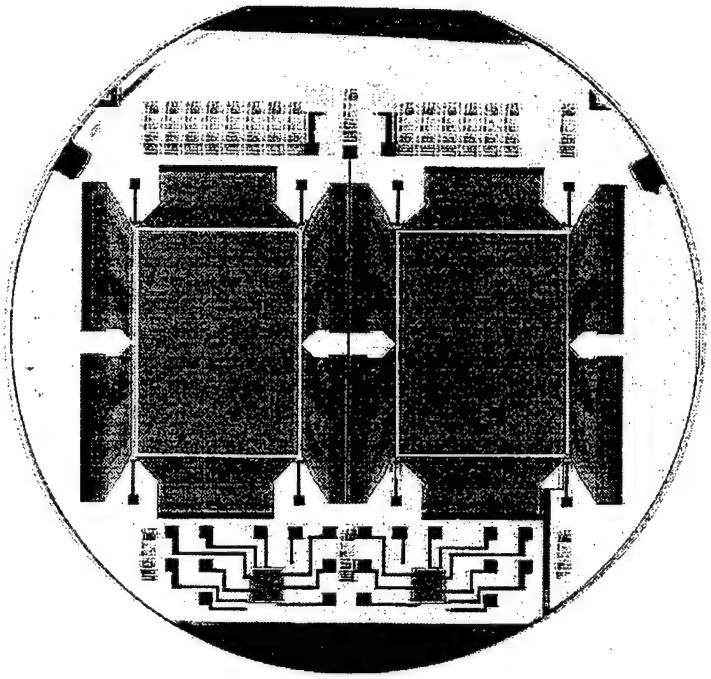


Figure 2.10 Photograph of the completed AMOLED array.

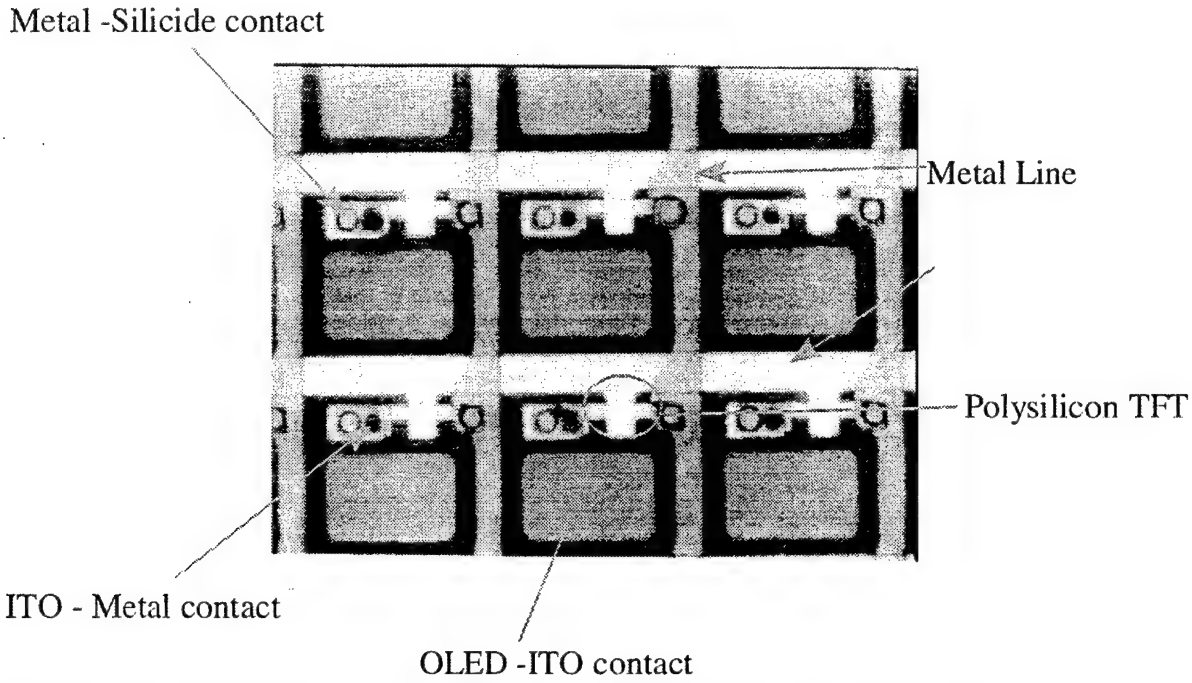


Figure 2.11 Photograph of a completed 50 μm square single TFT pixel (top view).

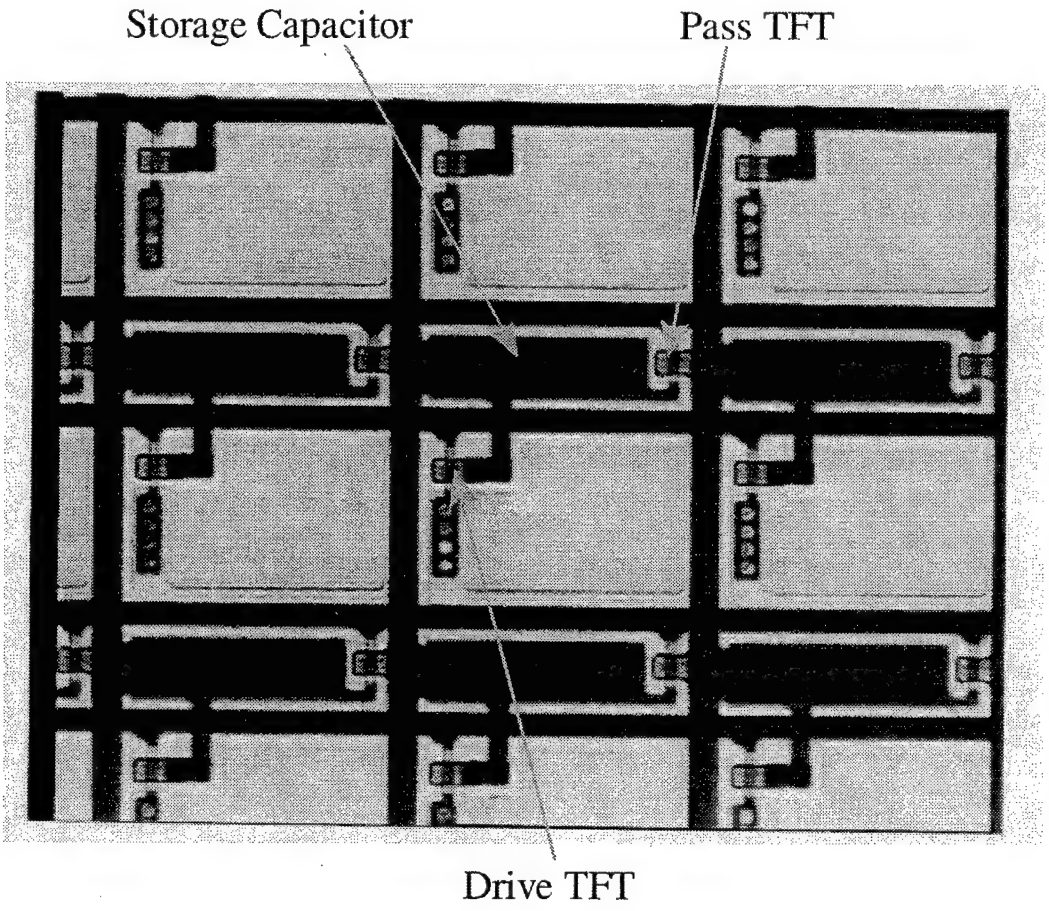


Figure 2.12 Photograph of completed 100 μm square pixel having the two-TFT design. The pass TFT, storage capacitor and drive TFT are indicated.

A unique driving method was implemented to operate the single TFT displays that were fabricated. Normally the address line turns on the gates of all the transistors in a line at once while maintaining the rest of the gates off. The data for this line is then written to the source of these pixel transistors. In our approach, we connect the address line to the source of all the pixel transistors, which is the data line in the other approach. The data is then written to the gates of the transistors. Figure 2.14 shows a schematic of both approaches. Figure 2.15 shows a photograph taken from a 4 cm VGA AMOLED display driven with this scheme.

The two-TFT-pixel design was tested for functionality. The testing was performed by illuminating alternating address lines. This method was chosen because illuminating alternate data lines does not demonstrate the sample and hold capability of the design. Good contrast was achieved indicating that this design has promise for active matrix OLED displays.

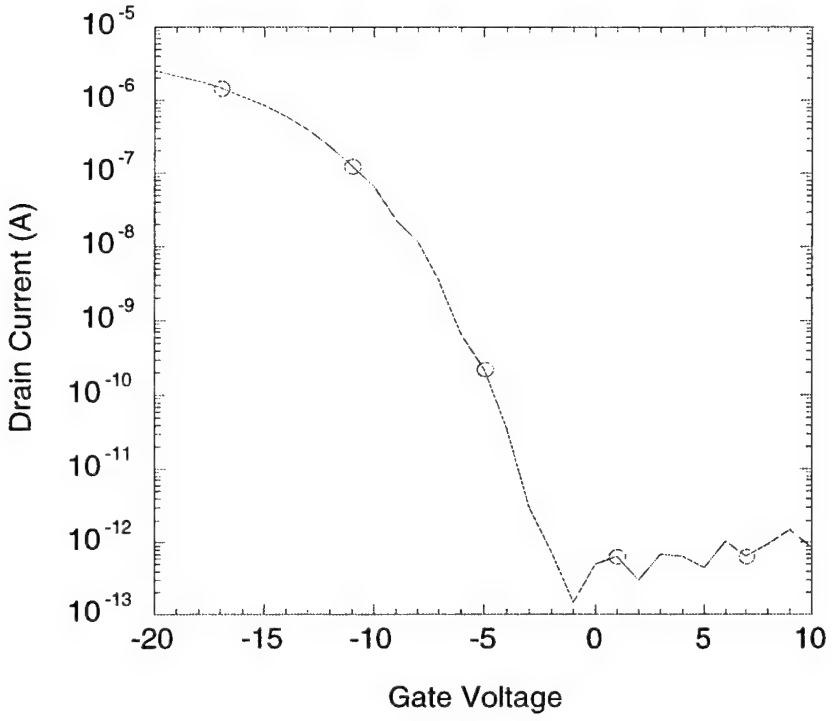


Figure 2.13 P-channel pixel TFT transfer characteristics. W/L= 4μm/8μm, V_{DS} = -1V.

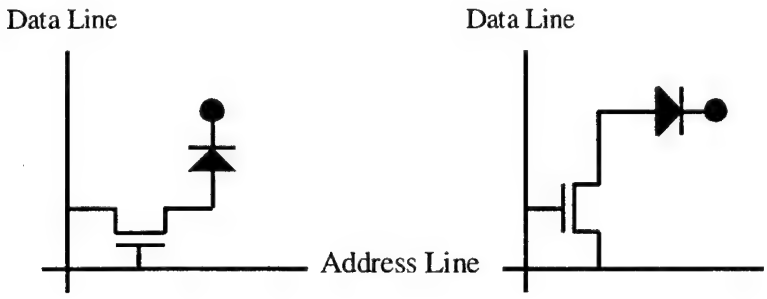


Figure 2.14 The schematic on the left illustrates the standard method of display driving. The gate of the TFT is used as the address line and an analog data voltage is written to the drain. Our method, shown on the right, connects the drain side of the TFT as the address line and writes the data voltages to the gates of the pixel transistors.

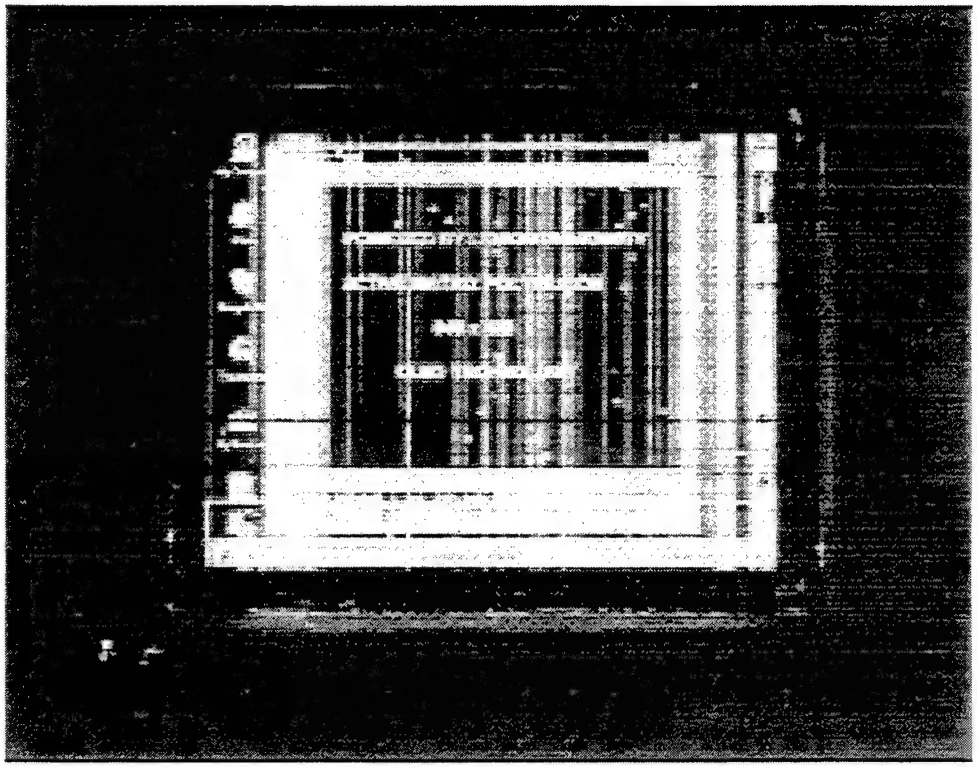


Figure 2.15 A 4-cm VGA polysilicon TFT based OLED display.

(The poor resolution is due to the digitization process)

2.5 Conclusions

A process to fabricate polysilicon TFT active matrix OLED display arrays has been described. In order to create a display with uniform brightness, a variety of steps have been introduced to reduce non-uniformity that may arise through processing. To achieve uniform transistor threshold voltage and carrier mobility, a solid-phase polysilicon crystallization by rapid thermal processing (RTP) was used. TFT threshold voltage variation less than 200 mV was achieved using the RTP crystallization process. To reduce the TFT series resistance, silicides were incorporated onto the source and drain regions of the TFT and the silicides were found to significantly improve TFT current uniformity. To reduce the series resistance of the pixel, a Ti-Al-Ni metallization scheme was developed to interface the ITO and the TFT island, resulting in a good ohmic contact to the ITO. The Ti-Al-Ni metallization scheme also eliminated hillocks, which could otherwise cause catastrophic shorts in the display. Finally, SOG was integrated to provide a well-planarized surface for the OLED material. The final array pixel TFTs had effective mobilities of 46 cm^2/V-s for n-channel TFTs, and 21 cm^2/V-s for the p-channel TFTs. These arrays resulted in functional VGA AMOLED displays with brightness of 101 cd/m^2.

Chapter 3

Polysilicon TFT Display Driver Circuits

Throughout this project, considerable work was done on polysilicon display driver circuits. As it was discussed in Chapter 1, one of the main advantages of polysilicon TFT technology is to the ability to integrate the display driver circuits along with the active matrix array on same substrate. In this work we demonstrated polysilicon display driver circuits using the low cost, high throughput, RTP crystallization process. We have fabricated shift registers operating as fast as 20 MHz. We have identified a trade-off between the carrier mobility and the gain of operational amplifiers. We have also developed a novel shift register design.

The first section discusses our results concerning polysilicon display driver circuits fabricated using the RTP crystallization process. The second section describes the performance of a novel shift register design. The third section details an interesting phenomenon that we observed which was the trade-off between the transistor mobility and the gain of operational amplifiers.

3.1 Characteristics of Low Temperature Polysilicon TFT Circuits

Integrating display driver circuits onto an active matrix TFT display panel can lead to more rugged displays with lower system cost because of the reduction of the number of required external driver chips and display connections. If no drivers were integrated, the number of external connections for a color VGA format display would be 640x3 + 480 = 2400. When drivers are integrated this number can be reduced by more than an order of magnitude. The integration of driver circuits can either be suited to an analog display interface or a fully digital display interface. The analog display interface scheme utilizes buffers, shift registers, and steering gates as the critical circuit components. The fully digital approach requires digital-to-analog converters (DACs) as well as analog signal amplification (operational amplifier) in addition to the components required for the analog interface scheme [3.1]. Figure 3.1 shows a block diagram of the analog and digital display driver integration approaches.

In order to be compatible with the display active matrix array processing, the driver circuits need to be fabricated on a large area, and preferably lost cost substrate such as glass. Furthermore, the driver circuits should be fabricated with the same material as the pixel transistors in order to simplify the fabrication process. Polycrystalline silicon (polysilicon) TFTs are an excellent contender as the active pixel element for high resolution AMLCDs as well as for the emerging display technology of AMOLEDs [3.2,3.3]. Currently, the dominant method to produce polysilicon TFTs is to crystallize the amorphous silicon using an excimer laser. This technique can yield high performance transistors suitable for driver circuits, but due to the scanning nature of the laser crystallization process, the transistor properties are not uniform. Transistor uniformity is critical for pixel TFTs for AMOLED displays in particular [3.2]. Furthermore, the laser

process suffers from high cost and low throughput. For these reasons, an alternate crystallization method is desired.

A new crystallization process, known as RTP, has been explored to improve the transistor uniformity, cost, and throughput of the crystallization process [3.4, 3.5]. This technique operates by scanning panels underneath a linear lamp, which selectively heats the amorphous silicon film compared to the substrate. Though the resulting transistor properties are highly uniform, the absolute transistor performance is not as high as that achieved using the laser crystallization process. Previous work has demonstrated low temperature polysilicon driver circuits using lower throughput furnace crystallization techniques [3.1, 3.6], but work needs to be done to determine whether or not the higher throughput RTP crystallization process is adequate for fabricating integrated driver circuits for active matrix displays.

The objective of this work is to demonstrate the functionality of the necessary components of integrated drivers in RTP crystallized polysilicon. These components include buffers, shift registers, operational amplifiers, and DACs.

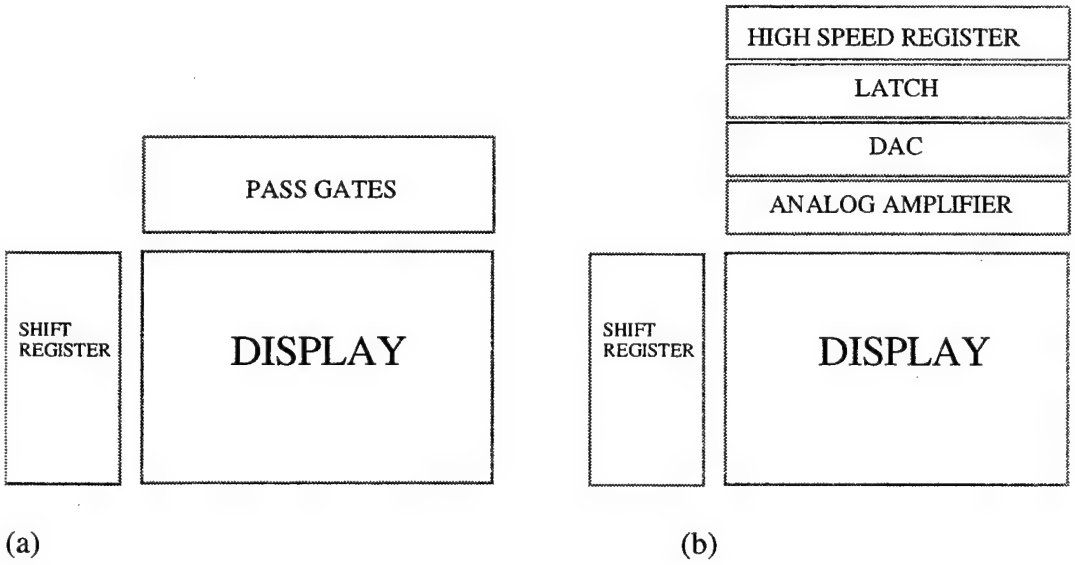


Figure 3.1 Block diagram indicating a display with integrated drivers having (a) an analog interface and (b) a digital interface.

3.1.1 Low Temperature Circuit Fabrication

Circuits relating to display drivers were fabricated at glass compatible temperatures on 100 mm quartz substrates using an RTP crystallization process. The silicon was deposited in the amorphous phase by PECVD deposition and then crystallized into polycrystalline silicon using RTP. The crystallization temperature was a strong function of the amorphous silicon deposition and annealing conditions. After optimization of these conditions, a crystallization temperature of the polysilicon as low as 640° C was achieved at a RTP scan speed of 5 mm/s [3.5]. This is less than the strain point of Corning 1737 glass. A self-aligned TFT process was used which incorporated the use of silicides to improve the

performance and uniformity of the transistors and the circuits. To verify the impact of silicides on circuit performance, a wafer was processed with only half of it being silicided. This enabled a direct comparison of the silicided and non-silicided circuits. The n-channel transistors had an average mobility of ~15.0 cm^2/V-s while the p-channel transistors had an average mobility of ~11.0 cm^2/V-s. The TFT drive currents were uniform within 5% for 90% of the tested device population.

3.1.2 Design of Polysilicon TFT Driver Circuits

To demonstrate the capability of RTP crystallized polysilicon for integrated drivers necessary integrated driver components for both an analog and a fully digital interface scheme have been designed. These components are buffers, shift registers, operational amplifiers, and digital to analog converters. First, the design issues regarding these components will be discussed. This will then be followed by a discussion of the performance of the various driver circuit components fabricated in the RTP crystallized polysilicon material.

3.1.2.1 Diagnostic Circuits - Ring Oscillators

Diagnostic circuits can be used to determine the maximum possible speed of a logic gate fabricated with RTP crystallized polysilicon TFTs. A ring oscillator consists of an odd number (N) of inverter gates connected back to back in a ring. This ring will oscillate with a period equal to N gate propagation delays. The ring oscillators used in this study contained 19 CMOS gates. Each inverter consists of a NAND gate with its two inputs connected together. This W/L ratio of the n channel TFTs and the p-channel TFTs was 20μm /4μm. A schematic of the ring oscillator is shown below in Figure 3.2.

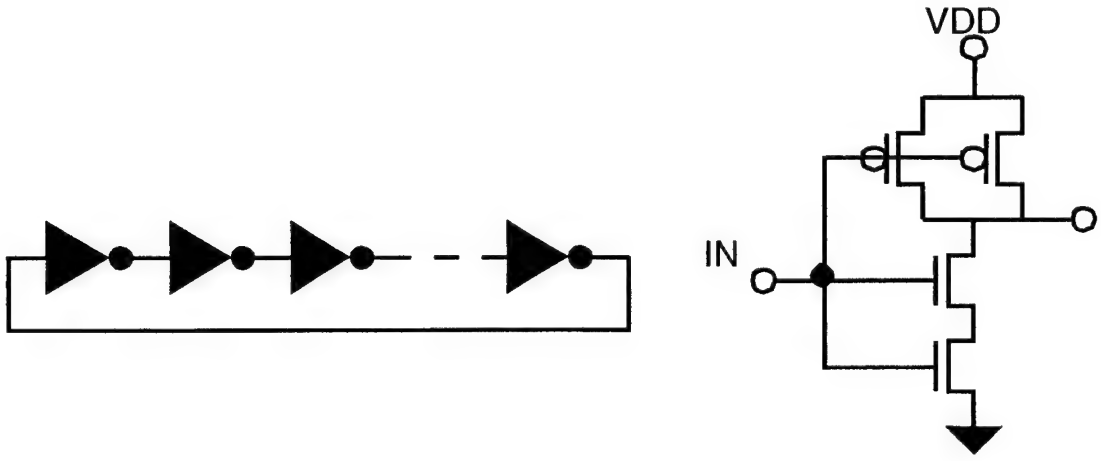


Figure 3.2 This figure shows the ring oscillator structure on the left and the internal inverter structure on the right.

3.1.2.2 Buffers

A buffer is useful in reducing the output impedance of a digital circuit as well as in isolating that circuit from its load. In the case of display drivers, the buffer is used to isolate the shift register and the address lines. This isolation is required to prevent a defect in the display or the buffer from adversely affecting the shift register operation and to prevent the capacitance of the display address line from slowing down the shift register. The buffer transistors need to be designed with large enough W/L ratios to drive the capacitive load of the address lines.

In this work, both NMOS and CMOS buffers have been characterized to determine their rise times for a 30 pF load. Each buffer contains four stages with the NMOS stages having W/L ratios of 20, 45, 90, and 180 and the CMOS stages having W/L ratios of 10, 25, 50, and 100. For the NMOS buffers, the saturation load TFT has a W/L ratio of 1/10 that of the drive TFT. The channel length was eight microns for all buffer TFTs.

3.1.2.3 Shift Registers

Multiple shift register architectures were investigated to determine which designs are most compatible with the properties of the RTP crystallized polysilicon transistors. Table 3.1 summarizes the designs that were investigated including some of the important features of each design. The designs are divided into three categories, static, dynamic, and pseudo-static. A static register relies on latches and will retain its digital information for an unlimited amount of time provided the power supply remains on. The dynamic designs rely on the pass transistor to hold a voltage at the input of an inverter while the clock is OFF. The leakage current of the pass TFT is critical for the dynamic designs. The slower the clock frequency, the more time the pass TFT has to leak. The dynamic designs will have a minimum frequency below which the register will not operate. The pseudo-static design provides a clocked feedback to prevent leakage of the pass TFT from affecting the output. However, the pass TFT will still leak during the time between clocks and this will lead to a maximum tolerable time between clocks after which the register will fail to operate. This is why it is labeled "pseudo-static." Figures 3.3 and 3.4 show the design schematics of these three approaches. The dynamic approach has the lowest transistor count (five per stage), which can lead to higher yield. The static design, an NMOS design based on clocked D Flip Flops (DFFs), requires eight transistors per stage but does not require low leakage current transistors. The pseudo-static designs require six TFTs per stage. The static and CMOS dynamic designs were not buffered and could be tested only up to speeds such that they could drive the input capacitance to the probe. The other designs were buffered and the W/L ratio of the final stage is also given in Table 3.1.

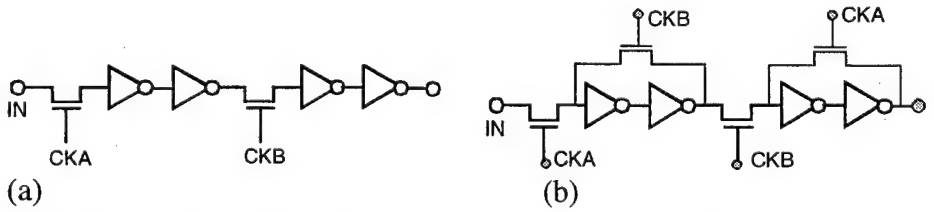


Figure 3.3 Circuit schematics of the (a) dynamic design and (b) pseudo-static design.

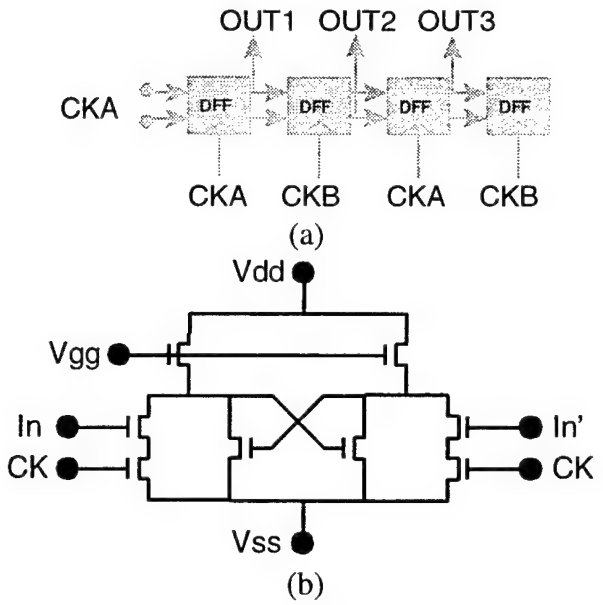


Figure 3.4 Schematics of the static shift register design showing (a) the block diagram and (b) the DFF internal circuit schematic.

Design		Technology	TFTs per Stage	Cell Pitch	Pass TFT W/L (um)	Buffer W/L
Static	D Flip-Flop	NMOS	8 T	70 um	x	x
Dynamic	Inverter Chain	CMOS	5 T	48 um	(80 / 8)	x
		NMOS	5 T	48 um	(12 / 4)	180,18
		NMOS	5 T	48 um	(12 / 4 (offset))	180,18
Pseudo-static	Inverter Chain	CMOS	6 T	36 um	(20 / 4)	50,50
		NMOS	6 T	48 um	(12 / 4)	30,3

Table 3.1 Overview of shift register designs to be investigated.

3.1.2.4 Operational Amplifier Design

An operational amplifier design was desired with maximum gain and minimum complexity to demonstrate the feasibility of op-amp design with RTP crystallized polysilicon TFTs. The design chosen was a CMOS uncompensated design containing nine TFTs. Figure 3.5 shows a circuit schematic of the op-amp [3.7]. The design consists of a differential amplifier stage, a level shifting stage, and a gain stage. The two input TFTs were chosen with a W/L ratio of 50μm /10μm. The 10 μm channel length was chosen to provide better saturation TFT behavior. The width to length ratio of the output stage is 50.

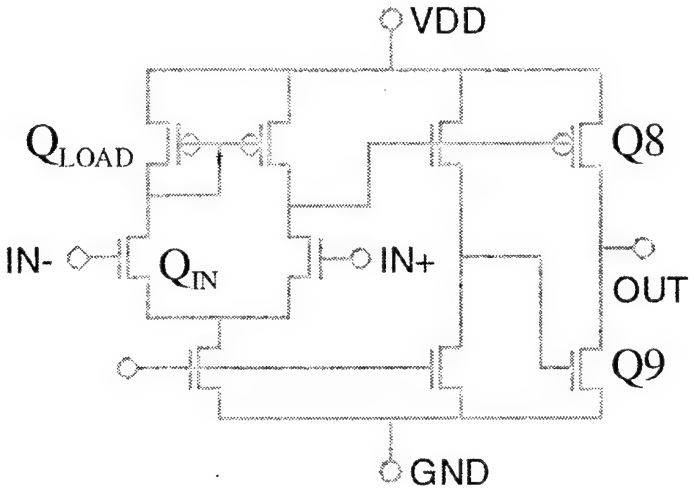


Figure 3.5 Uncompensated operation amplifier schematic [3.7].

3.1.2.5 Digital to Analog Converter Design

Our goal in the design of the DAC was to achieve proper digital to analog conversion with the simplest design. For these reasons a current-based DAC architecture was used. Low transistor count is critical in large area electronics where yield is an important issue. This design, shown in Figure 3.6, requires four transistors for three-bit conversion and would require one additional TFT for each additional bit of resolution. Of the four transistors, the load TFT (transistor at the bottom of the schematic) is intended to operate in the linear mode and serve as a fixed value resistor. The widths of the input transistors, A, B, and C, are N, 2N, and 4N respectively. If the resistance of the load TFT is small, these transistors will have approximately the same V_{DS} and therefore will deliver a current proportional to their widths when its input bit is high (V_{HIGH}). The output voltage of the DAC equals the sum of these currents multiplied by the resistance value of the bottom TFT. This formulation is given in equation (1), where it is assumed that the input TFTs are operating in saturation.

$$V_{OUT} = I_{Total}R = (4I_0A + 2I_0B + I_0C)R$$
$$= (4A + 2B + C)(\frac{W}{L}\mu C_{ox}(V_{HIGH} - V_{TH})^2)(\frac{W_{Load}}{L_{Load}}\mu C_{ox}(V_{GG} - V_{TH}))^{-1} \quad (1)$$

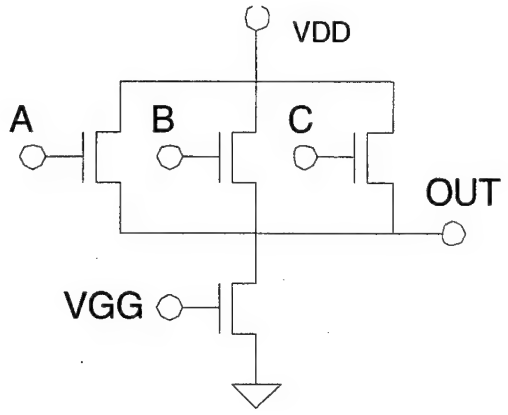


Figure 3.6 Current based three- bit DAC design.

3.1.3 Experimental Characterization of Polysilicon TFT Circuits

3.1.3.1 Diagnostic Circuits

The oscillation period of the ring oscillators were characterized as a function of the power supply voltage. Figure 3.7 plots the delay per gate as a function of the supply voltage. At a supply voltage of 26 V, a gate delay as low as 5 ns was achieved. This indicates a maximum circuit frequency of 100 MHz. This speed is above what is required for integrated display drivers for VGA sized displays. A calculation of shift register speed requirements is found in Appendix B. Figure 3.7 also illustrates the difference between using silicided devices and low resistance silicided gate interconnects compared with using a standard highly doped polysilicon gate process. It can be seen that the silicidation process improves the circuit speed by approximately 10%.

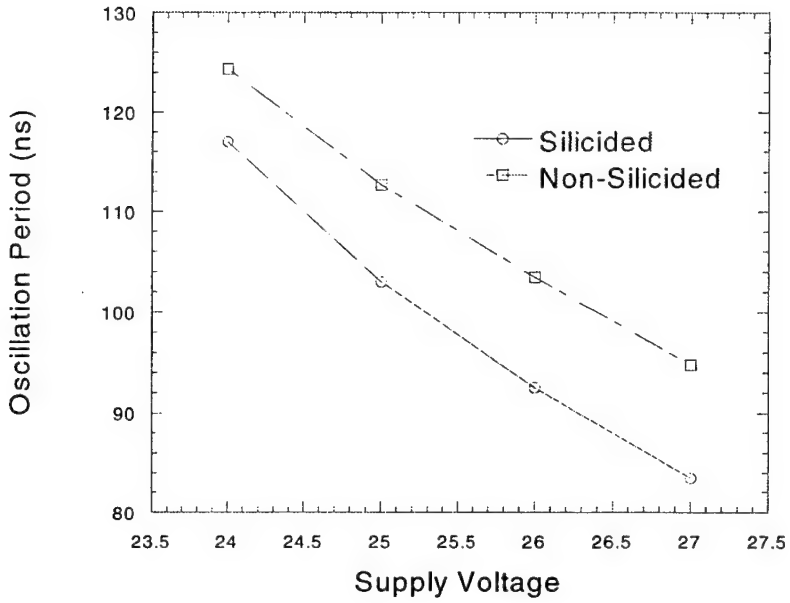


Figure 3.7 Oscillation period of a 19-stage ring oscillator as a function of the power supply voltage. The data is shown for both silicided and non-silicided ring oscillators.

3.1.3.2 Buffer Characterization

Both the NMOS and CMOS buffers were tested to determine their rise and fall times. A 30pF load was used. Figure 3.8 plots the rise and fall times of the two buffer technologies as a function of the supply voltage. The expected trade-off between operating speed and supply voltage is evident. Also as expected, the NMOS technology consumed far more power than the CMOS technology for the same rise time (2 mW/stage compared to 0.001 mW/stage for V_{DD}=20V). However, the CMOS technology required higher operating voltages to achieve microsecond rise and fall times (30V compared to 22V). This is due to a higher p-channel TFT threshold voltage compared with the n-channel TFT threshold voltage for the low temperature RTP crystallized material.

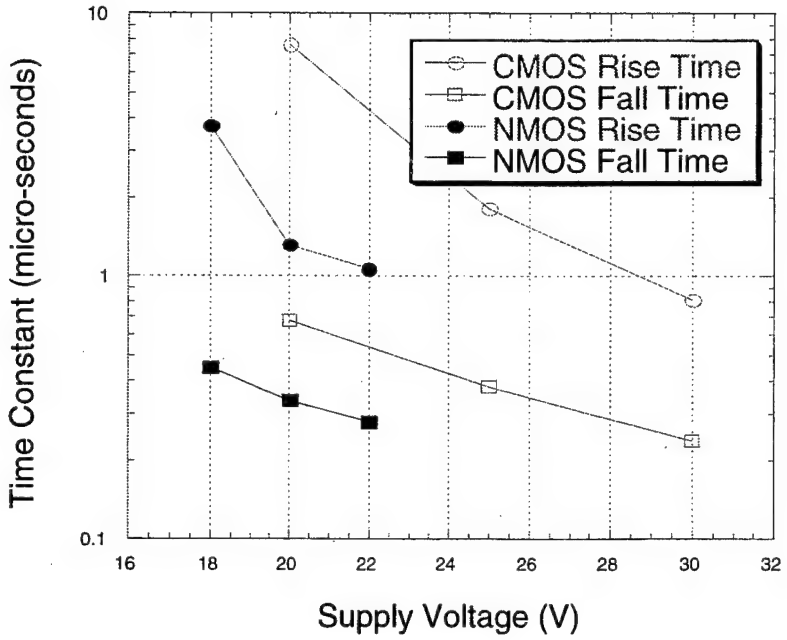


Figure 3.8 Rise and fall times of NMOS and CMOS buffers. C_{LOAD} = 30 pF

3.1.3.3 Shift Register Characterization

The designs listed in Table 3.1 were fabricated and characterized and their performance is summarized in Table 3.2. The first column lists the supply voltage for which the register was tested and the second column lists the DC power consumed. The minimum operating frequency is the minimum speed that the register could be functionally driven. This parameter provides insight into the leakage current of the pass transistors. The lower the TFT-leakage current, the lower the minimum operating frequency. It can be seen from Table 3.2 that the NMOS dynamic design using offset devices (TFTs optimized for lower leakage current) has a lower minimum operating frequency than the same design using the standard self-aligned TFT structure. All designs were tested using a clock high voltage of 15 V and a clock low voltage of 0 V.

Table 3.2 also shows the results of two different methods used to measure the maximum speed of the shift register. Method A lists the maximum sucessfully tested frequency. However, this parameter is dependent upon the high frequency clock generation limitations of our equipment (~5 MHz). Furthermore, the output waveforms are distorted at higher frequencies due to the load capacitance of the measurement set-up and the size of the buffer output stage. To overcome these testing limitations, the results of a second method are also listed in Table 3.2 under the column, Maximum Frequency - B. This technique measures the minimum clock pulse width applied to the pass gates for the register to maintain proper shifting operation. This time was measured by varying the duty cycle of the clocks at frequencies lower than the maximum speed of the register.

This minimum clock pulse width provides an indication to the maximum speed of the register, according to equation (2), without requiring the buffer to switch at that speed.

$$f_{MAX} = \frac{1}{2 * \tau_{MIN}} \tag{2}$$

It can be seen from Table 3.2 that all of the designs except for the static design are able to operate in the MHz frequency range. The results of the two maximum frequency measurement techinques are consistent for those cases where the maximum frequency is less than the maximum testing frequency of the set-up (2.5 MHz). In the cases where the registers were still operating at 2.5 MHz, the second technique provides the only measurement of the maximum register speed. The speed limitation of the dynamic and pseudo-static designs is likely due to the limitation of the pass transistors ability to adequately charge the next stage in the clock time. If the clock voltage is reduced below the 15 V standard used during the measurements presented in Table 3.2, the maximum speed of the register is reduced, indicating that the conductance of the pass transistor does indeed limit the maximum register speed. If the pass TFTs were designed with a greater W/L ratio, the register would operate at higher frequencies. The static design speed limitation can be attributed to the small W/L ratio of the load TFTs of the DFFs. Increasing the W/L ratio of this TFT should increase the maximum speed of this register.

Figure 3.9 shows the timing diagram for the dynamic NMOS register (48 μm pitch) operating at a clock frequency of 30 kHz. This is the required speed for a shift register as an integrated scan driver for a VGA sized display operating at 60 frames per second. The non-overlapping clocks are shown as well as the input and the outputs of the 2nd, 4th, 6th, and 8th stages with relation to the input signal. It can be seen that the subsequent stages are each properly shifted by one clock cycle.

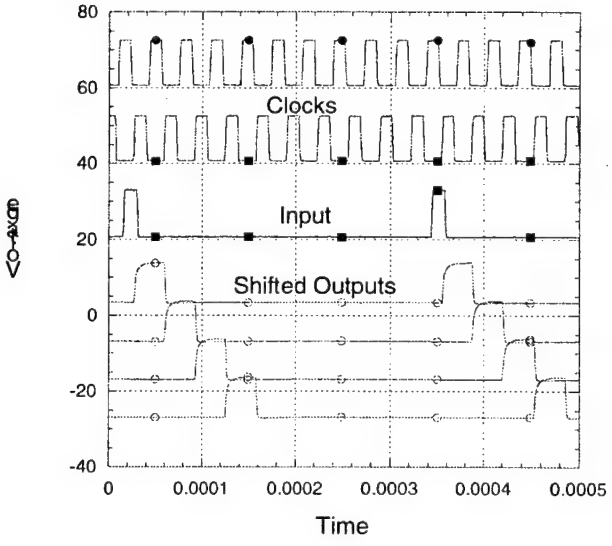


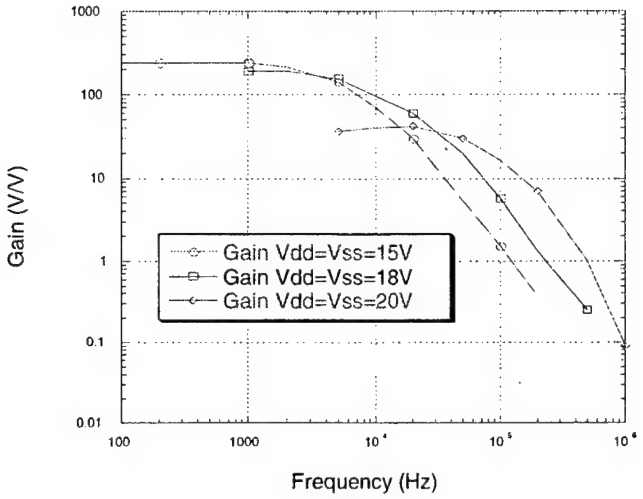
Figure 3.9 Timing diagram showing the shifted outputs of a dynamic NMOS register operating at 30kHz. The two clocks, outputs and the input are shown.

Design		Technology	Supply Voltage	Minimum Speed	Maximum Speed - A	Maximum Speed - B	DC Power / Stage
Static	D Flip-Flop	NMOS	20	x	50 kHz	62.5 kHz	1.3 mW (unbuffered)
Dynamic	Inverter Chain	CMOS	20	18 kHz	> 2.5 MHz	17 MHz	0.019 mW (unbuffered)
		NMOS	20	230 kHz	1.4 MHz	1.7 Mhz	16 mW
		NMOS(offset)	20	100 kHz	2 MHz	1.4 MHz	16 mW
Pseudo-static	Inverter Chain	CMOS	20	250 kHz	> 2.5 Mhz	20 MHz	0.13 mW
		NMOS	20	180 kHz	> 2.5 MHz	12.5 MHz	1.8 mW

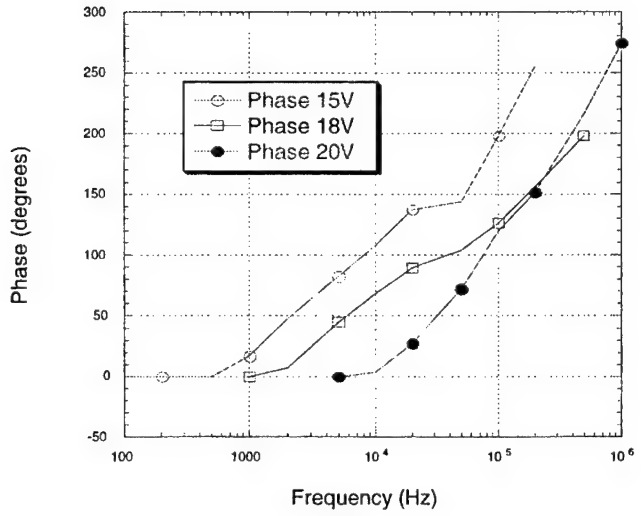
Table 3.2 Summary of shift register performance.

3.1.3.4 Operational Amplifier Characterization

The CMOS operational amplifier design was fabricated and characterized for both AC and DC performance. Figures 3.10(a) and 3.10(b) show the AC performance of the op amp at different supply voltages. The unity gain point for the design is greater than 200 kHz for a supply voltage of 15 V and increases with increasing supply voltage.



(a)



(b)

Figure 3.10 This figure shows the (a) gain and (b) phase plots for the uncompensated operational amplifier with Vdd=Vss=18 V. The W/L ratio of the CMOS output stage = 50 and C_{LOAD} = 30 pF.

It can be seen the higher supply voltages increase the unity gain frequency as well as increase the frequency for which the output is 180 degrees out of phase with the input. The op amps had a maximum DC gain of 500 (54 dB) depending upon the polysilicon material properties. This effect will be discussed in more detail later in this report.

3.1.3.5 Digital-to-Analog Converter Characterization

The DAC design was fabricated and tested for functionality at low frequencies. Figure 3.11 plots the output voltage of the DAC as a function of time. The three input bits were varied with time to raster from the case of the digital inputs being all high to the case of the digital inputs being all low. The bits were changed at a frequency of 1.2 kHz. This sequence was then repeated in time at a frequency of 150 Hz. The output voltage range of the DAC was between 0 and 0.5 volts. This smaller range can be amplified to the desired range using analog amplification methods, such as an op-amp.

It can be seen from Figure 3.11 that the output is not completely linear with the input bit sequence. This is because the resistance of the amount of current flowing through the input transistors is a function of their gate to source voltages. The source voltage depends directly upon the output voltage of the DAC. If the output voltage changes are small, the linearity can be improved. This can be accomplished by reducing the resistance of the load TFT by increasing the voltage on its gate (Vgg). The linearity of the design also may be improved by using p-channel TFTs as the input transistors. If operating in saturation, this eliminates the dependence of the input TFT current on the output of the DAC.

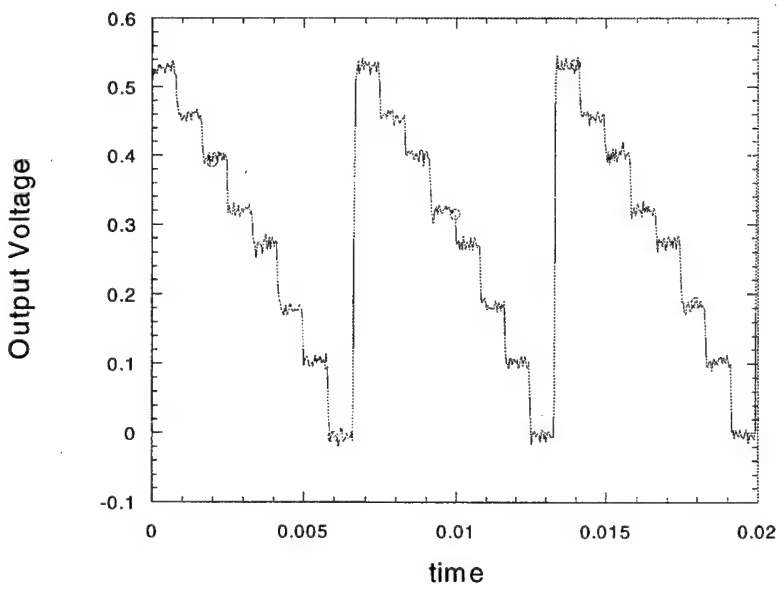


Figure 3.11 Plot of DAC output voltage as a function of time. The input bits are changed at a rate of 1.2 kHz.

3.2 A Novel Shift Register Design

Polycrystalline silicon (polysilicon) has emerged as the leading deposited semiconductor candidate for high resolution AMLCDs and AMOLED displays where integrating driver circuitry has the greatest benefit [3.8, 3.9, 3.10]. Polysilicon TFTs can be fabricated at temperatures less than 650° C but there remains a trade-off between device performance and polysilicon deposition and crystallization cost and throughput. Prior methods to achieve high quality polysilicon devices resulted in either low throughput, such as furnace anneal, or high equipment cost, such as the excimer laser anneal. Low cost, high throughput crystallization methods such as RTP have been recently proposed but the device performance is not as good as the laser-crystallized material [3.11]. As a result, the design of integrated driver circuits for low temperature polysilicon technology must be as forgiving as possible to accommodate variable levels of transistor performance. This work discusses a dynamic shift register design with an improved range of operating frequency. The increased range of operating frequency relaxes the constraints on the TFT performance and therefore is a better design particularly for high throughput, low cost polysilicon technology.

The shift register is an important circuit component for integrated drivers. Shift registers can be used as the address line circuit to activate each display row line in sequence. The shift register can also be used to load serial digital data into a parallel display data driver latch [3.12]. The speed requirement of a shift register operating as an integrated address circuit is approximately 30 kHz for a VGA format display operating at 60 frames/second. However, the operating speed will increase as the number of gate lines or as the frame rate increases. The operating frequencies of a shift register being used for data loading functions are much faster (>1 MHz) depending on how many digital inputs the display is using as well as on the display format. For either application, it is desirable to have a shift register design that can function over as broad a frequency range as possible.

Shift registers can be designed in both static and dynamic modes. Though static designs have no lower limit on operating frequency, they require more transistors per stage than does a dynamic register design. For large area electronics applications, it is desirable for the shift register to have as few transistors as possible in order to increase the fabrication yield. Since yield is an important concern, the dynamic register architecture is of great interest for integrating display driver circuits onto large area substrates.

A common version of a dynamic shift register design is shown in Figure 3.12. The design is based on a chain of inverters that are separated by pass gates which are clocked with opposite non-overlapping clock phases. This dynamic design has a maximum operating frequency and a minimum operating frequency that is dependent largely upon the properties of the pass TFT. It is desired to have a maximum frequency as high as possible and a minimum frequency as low as possible in order to have the greatest range of register operation.

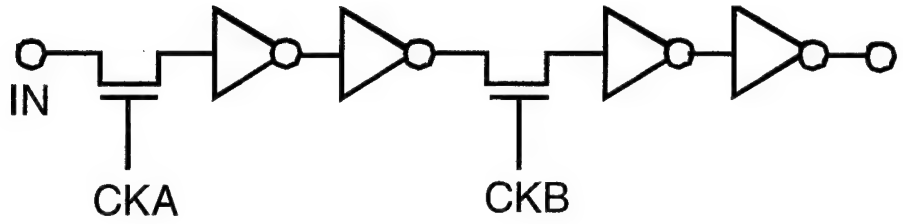


Figure 3.12 Dynamic shift register schematic

The maximum frequency is limited by the ability of the pass TFT to charge the input capacitance of the next buffer within the time period of the clock. The more conductive the pass TFT is when its clock is high, the higher is the maximum frequency of the register. The leakage current of the pass TFT determines the minimum frequency. The charge stored on input capacitance of the next inverter will leak through the pass TFT until that inverter changes states. When that happens, the register is in error. Therefore, the transistor structure of the pass TFT is critical in determining the frequency limitations of the register.

The pass gate TFT can be fabricated using a variety of TFT structures. The most common polysilicon TFT structure is the self-aligned structure. A device cross section of the self-aligned TFT is shown in Figure 3.13(a). The self-aligned TFT structure minimizes the series resistance of the TFT and maximizes its ON current. A shift register using this device structure will maximize its maximum operating frequency. However, due to the high leakage current of the self-aligned polysilicon device, the minimum operating frequency of the register may be too high for it to operate properly as a display address line driver circuit. To reduce the minimum operating frequency of the register, the leakage current of the polysilicon pass gate needs to be reduced. The most common device structure used to accomplish this in the LDD structure [3.13], shown in Figure 3.13(b). In this structure, the channel is separated from the heavily doped, low resistance source and drain regions with a lightly doped, high resistance region. This region reduces the electric fields at the drain when the TFT is OFF and, as a result, reduces the leakage current of the TFT compared with the self-aligned structure. However, due to the introduction of the lightly doped region in series with the TFT, the ON current is reduced as well.

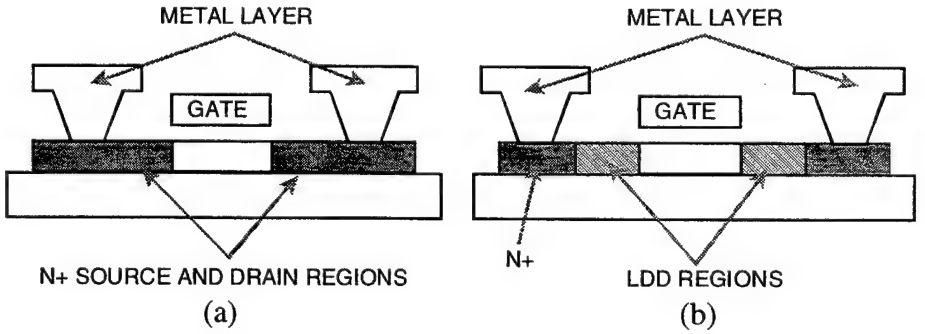


Figure 3.13 Cross sections of (a) self-aligned TFT structure and (b) LDD TFT structure

A dynamic shift register using a LDD pass gate TFT structure will have a reduced minimum operating frequency compared with using a self-aligned pass gate TFT structure, but at the expense of also having a reduced maximum operating frequency. In this work we investigated a different pass gate TFT structure to improve the operating frequency range compared with either the self-aligned or LDD TFT structures. The structure consists of a modified LDD pass TFT structure, but with the addition of a second control gate that is used to modulate the conductivity of the lightly doped regions of the LDD device. When a positive bias is applied to the control gate, the concentration of carriers in the LDD regions is increased. This extra terminal can provide an increase in the ON current of the device without sacrificing the low leakage current behavior of the LDD structure. This operation of this device is similar to other device structures aimed at increasing the concentration of carriers in the LDD region [3.14,3.15]. A cross section of this device structure is shown in Figure 3.14.

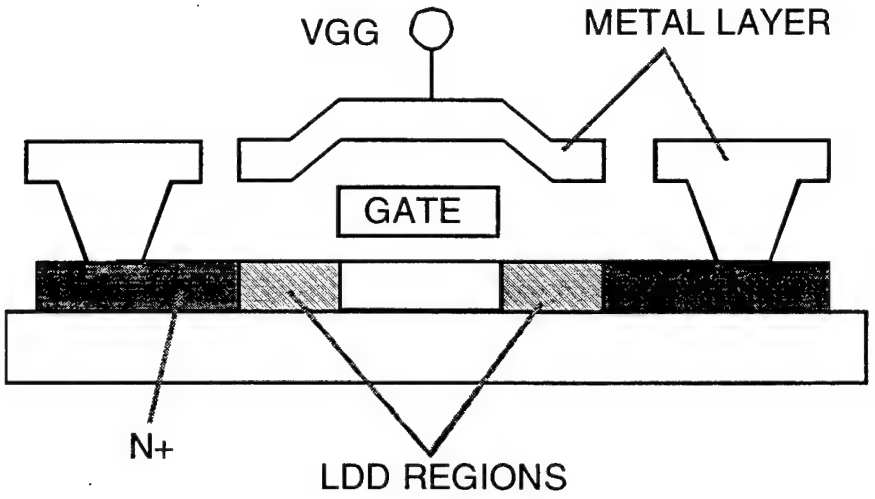


Figure 3.14 Cross section of modified pass gate TFT structure

3.2.1 Fabrication

Dynamic shift registers with the different pass TFT structures indicated in Figures 3.13(a) and 3.13(b) were fabricated on 100 mm quartz substrates. Amorphous silicon was deposited by PECVD and then crystallized using the high throughput RTP crystallization process. Crystallization temperatures of the polysilicon were less than the strain point of Corning 1737 glass. A 100 nm gate dielectric was then deposited using PECVD followed by the in-situ deposition of an amorphous silicon gate. Source and drain doping was achieved by ion implantation of phosphorus with a dose of $2x10^{15}$ cm^{-2}. The LDD regions of the n-channel TFT were also doped by ion implantation of phosphorus but with a dose of $5x10^{12}$ cm^{-2}. The dopants were activated in a furnace at 650^{o} C. This was the maximum temperature of the process. After activation, 300 nm of PECVD passivation oxide was deposited followed by contact holes and metallization. The metallization layer was used for the second gate of the new pass TFT structure.

The self-aligned n-channel transistors had an average mobility of 15 cm^2/V-s. Figure 3.15 plots the transfer characteristics of the standard LDD (V_{GG}=0V) and the gated LDD structure. The characteristic of a self-aligned TFT is shown for comparison. It can be seen that the gated LDD device has a greater ON-OFF ratio compared to the standard LDD device and therefore is expected to lead to a greater range of operating frequency when applied to the dynamic register design.

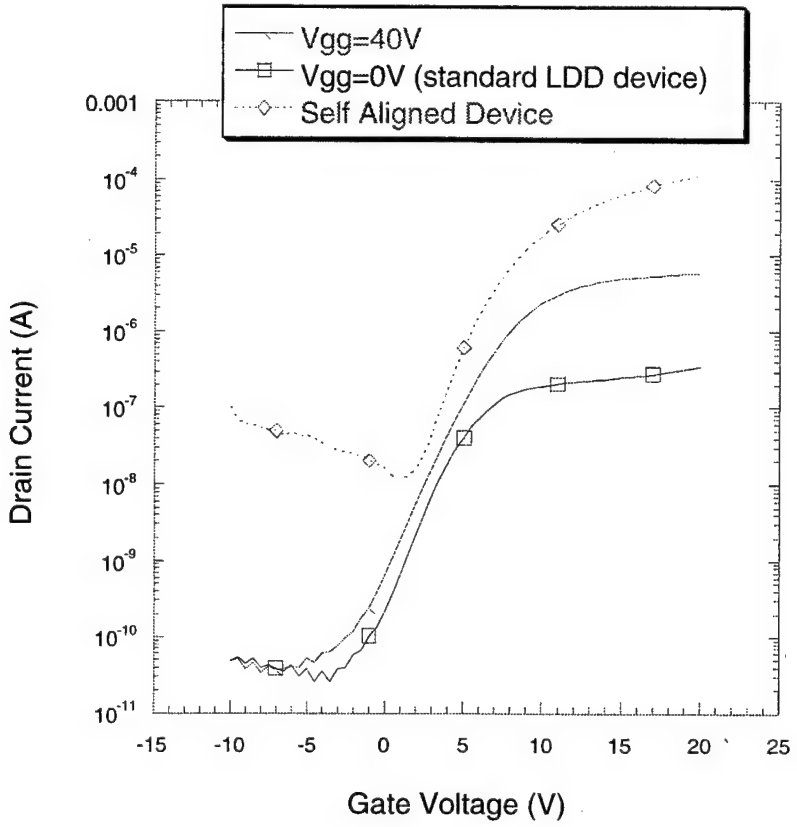


Figure 3.15 Transfer characteristics of the standard LDD structure (V_{GG}=0V), gated LDD structure, and self-aligned TFT structure.

3.2.2 Characterization

The dynamic registers with the different pass TFT structures behaved as expected with respect to their minimum and maximum operating frequencies. Figure 3.16 plots the minimum and maximum frequency of the dynamic shift register design as a function of the gate voltage over the LDD (V_{GG}) regions. All registers were tested for V_{DD}=17V. The standard LDD structure is equivalent to the case where V_{GG} = 0V. According to Figure 3.16, the standard LDD device achieved the lowest minimum operating speed of 500 Hz, but the increase of the minimum speed with increasing V_{GG} was minor. Even for V_{GG} = 40 V, the minimum operating frequency has only increased to 730 Hz. However, the increase in maximum frequency with increasing V_{GG} was far more significant. The

maximum operating frequency of the register using the standard LDD structure (V_{GG} = 0 V) was 49 kHz while the maximum operating frequency for the case of V_{GG} = 40 V was 333 kHz.

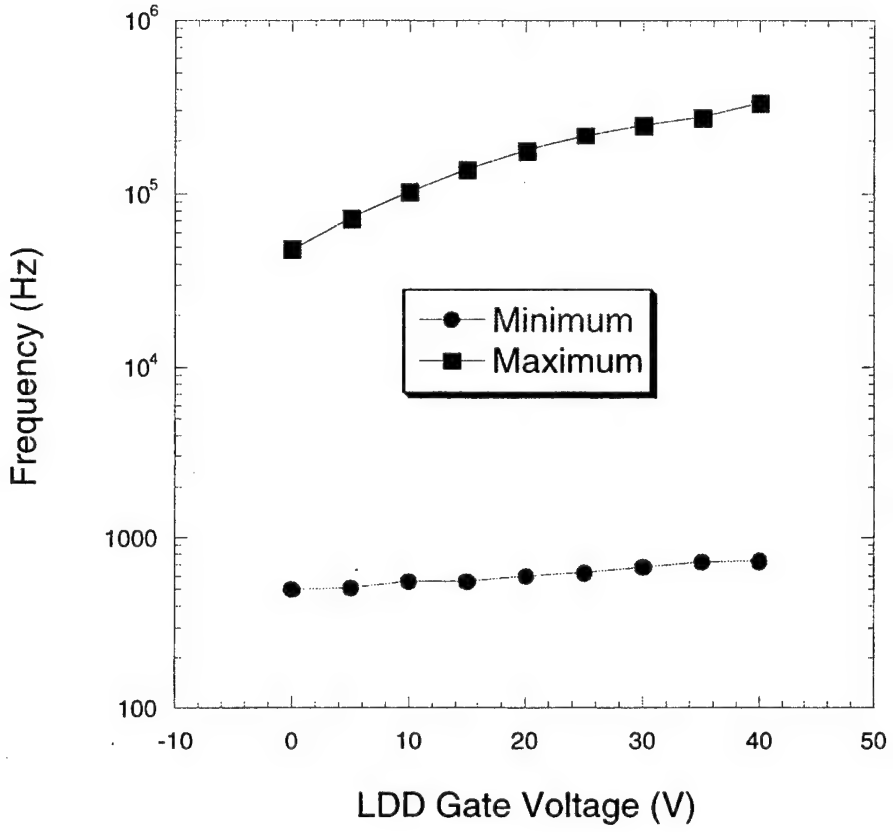


Figure 3.16 Plot of the minimum and maximum frequency for the dynamic as a function of V_{GG}. The register with V_{GG} = 40 V has the greatest range of operating frequency.

Since the increase in maximum operating frequency was far greater than the increase in the minimum operating frequency, the register with V_{GG} = 40 V has a much greater range of operating frequency than the register using the standard LDD pass gate structure. Figure 3.17 plots the operating range of frequency (f_{MAX}/f_{MIN}) as a function of the LDD gate voltage (V_{GG}) voltages. It can be seen that the gated LDD structure has a factor of five greater operating frequency range compared to the standard LDD device (V_{GG} = 0V). Figure 3.18 shows the timing diagram of the dynamic register using the gated LDD structure operating at ~ 30 kHz. The design was buffered with an output W/L ratio of 180μm/8μm for the drive TFT and 18μm/8μm for the saturation NMOS load TFT. The non-overlapping clocks are shown as well as the input and the shifted outputs.

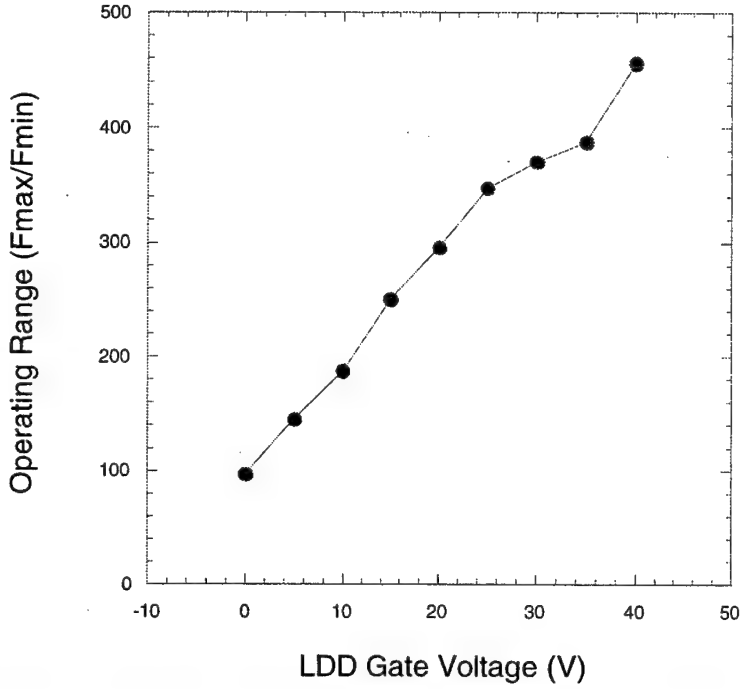


Figure 3.17 Operating frequency range as a function of the LDD gate voltage (V_{GG}).

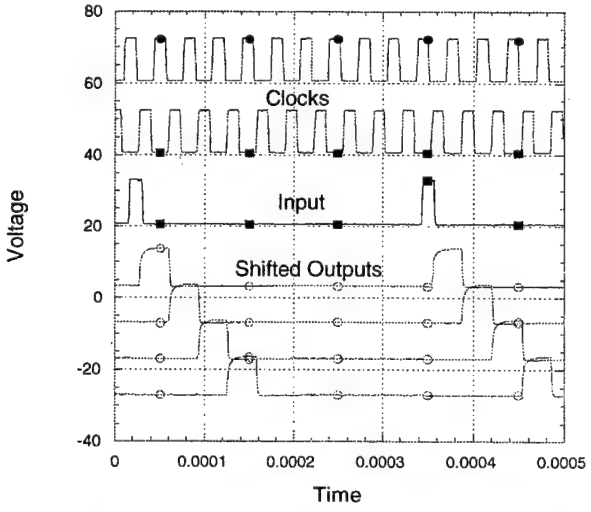


Figure 3.18 Timing diagram of an operating polysilicon dynamic shift register design. The register is operating at 30 kHz.

3.3 Trade-Off Between Carrier Mobility and Op-Amp Gain

This section describes a trade-off between the carrier mobility and the gain of an operational amplifier. In general, we wish to fabricate TFTs with high mobility and amplifiers with high gain. However, in this section we describe some of our results that indicate that these two goals are in conflict.

The theoretical gain of the op-amp that was investigated in this work is given by equation (1) [3.7]. It can be seen from equation (1) that the op-amp gain can be increased by increasing either the TFT trans-conductance or by reducing the TFT saturation conductance.

$$A = \left(\frac{-g_{mi}}{g_{dl} + g_{di}} \right) \left(\frac{g_{m8} + g_{m9}}{g_{d8} + g_{d9}} \right) \tag{1}$$

The CMOS operational amplifier design was fabricated and characterized for AC and DC performance. The AC performance was already presented earlier in Section 3.1. The op amps had a large variance in DC gain ranging from less than 100 to over 500 depending upon the polysilicon material properties. In general, the goal is to achieve as large gains as possible. In order to maximize the operational amplifier gain it is necessary to understand how the TFT performance impacts the DC op-amp gain. Equation 8 indicates that larger g_m and smaller g_d lead to increased DC op-amp gain. Polysilicon TFTs fabricated in larger grain size polysilicon are known to have higher mobility. Increasing the mobility increases the g_m and hence should increase the op-amp gain. However, we found that smaller grain sizes have a reduced g_d by reducing the channel length modulation effect and thereby also increase the op-amp gain. To investigate the effect of polysilicon microstructure on op-amp DC performance, operational amplifiers were measured for a variety of low temperature polysilicon materials having a variety of mobility values.

Figure 3.19 plots the DC open loop gain as a function of the carrier mobility at a supply voltage of 20 V. From this plot, it is clear that larger op-amp gain is achieved using polysilicon material with smaller mobility. Apparently, even though these materials have smaller g_m, they also have smaller g_d which leads to an increase in the open loop gain.

3.4 Conclusions

This work shows that RTP polysilicon is a viable material for integrating driver circuitry onto the display panel. Both digital and analog circuits, suitable for AMLCDs and AMOLED displays, have been demonstrated for the first time in RTP crystallized polysilicon material. Ring Oscillators indicate a maximum logic gate operation speed of 100 MHz at Vdd = 28 V. NMOS and CMOS buffers have been fabricated and tested to have rise and fall times less than 1 μs for a 30 pF load. Multiple shift register designs have been characterized, and operating speeds greater than 20 MHz were achieved. Functional DACs and operational amplifiers have also been demonstrated and an open loop gain as high as 500 V/V was achieved.

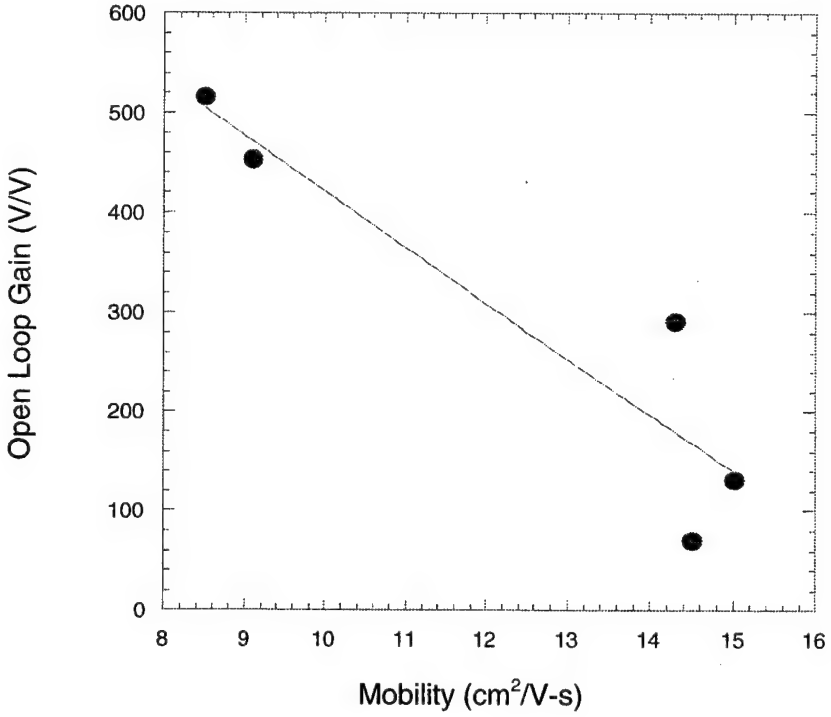


Figure 3.19 The DC open loop op-amp gain is plotted as a function of the polysilicon carrier mobility. Smaller mobility leads to larger open loop gains.

A design improvement for dynamic shift registers fabricated with low temperature polysilicon TFTs has been described. A greater range of operating frequency was achieved using a gated LDD device structure for the pass gate of the dynamic register (f_{MAX}/f_{MIN} = 450). This was more than four times greater than that achieved using a standard LDD pass gate structure (f_{MAX}/f_{MIN} = 100). This improvement in operating frequency range is explained by an increase in the ON current of the pass gate without a significant increase in the leakage current. This increase in operating frequency range is important to low temperature integrated display driver circuit design. The greater range of operating frequency provides more tolerance to limitations in device performance and indicates an improvement in register design. An analysis was also performed that related the carrier mobility and the gain of an operational amplifier. It was shown that a trade-off exists between high carrier mobility and high gain. It was shown that larger op-amp gain is achieved using polysilicon material with smaller mobility. Even though these materials have smaller transconductance, they also have smaller conductance, which leads to an overall increase in the open loop gain. This observation and understanding is important in optimizing the polysilicon material not only for device performance but also for circuit and system performance.

Chapter 4

Advances in AMOLED Array Metallization

In this chapter we discuss in detail the metallization processes that were developed and used to fabricate the AMOLED arrays discussed in Chapter 2. These processes include:

1) A low temperature silicidation method, in order to improve on current and uniformity of the polysilicon TFT devices.

2) A hillock-free, low resistance metallization scheme that could be used as the array interconnect level. Hillock-free is required to avoid shorts with the OLED cathode electrode while the low resistance to reduce the parasitic line resistance.

3) A metallization process that yields an ohmic contact with low contact resistance between the TFT and the transparent ITO pixel electrode of the OLED material

The following sections describe in detail the results in each of the above three areas. The first part deals with the effort to develop an AMOLED process compatible silicide. The second section is on the work that went into developing a hillock free metallization. The third and final section explains the development of an ohmic contact to an ITO electrode.

4.1 Cobalt and Nickel Silicides for Polysilicon TFTs.

Silicidation on thin (<100 nm) silicon films is useful for polysilicon AMOLED display applications because the thin film transistors exhibit high extrinsic series resistance [4.1.1]. Such silicidations need to take place at low temperatures, as the processing must be compatible with the use of glass substrates for AMOLEDs, which limits thermal processing to below 700° C [4.1.2]. Our work has showed that cobalt and nickel are compatible with polysilicon thin film transistor active matrix flat panel display processing.

Low temperature fabrication of thin silicides is also becoming a necessity in single-crystal silicon CMOS processing, because the decreasing junction depth requires the formation of thin silicides at temperatures which will not cause re-diffusion of shallow junctions. Cobalt and nickel form silicides at temperatures below that of titanium [4.1.3, 4.1.4]. In this work, cobalt and nickel silicides were investigated on polysilicon films with thickness variations ranging from 18 to 100 nm, and for comparison purposes, on single-crystalline silicon.

In CMOS circuit fabrication, a clean, dry, oxygen-free surface is required for reliable silicidation [4.1.5]. In this work we examined the role of surface preparation and drying method as well as the thickness of the polysilicon layer on the sheet resistance of the resulting silicide, expanding on previous work by Mishima et. al. [4.1.6, 4.1.7]. The

impact of these variables on the silicidation reaction was determined through the sheet resistance of the silicide. A method using isopropanol (IPA) drying to prepare clean, dry, passivated surfaces for the reproducible fabrication of silicides on large area glass substrates is presented. Furthermore, the silicides were tested to determine their chemical and thermal stability under normal process conditions. The silicon layers used in this study were 100 nm and 18 nm thick polysilicon films, and the resulting silicides were compared to that of "standard" samples of silicides formed on crystalline-silicon substrates.

4.1.1 Preparation of Silicides

4.1.1.1 General Deposition Conditions

The general preparation, deposition, and silicidation conditions are given in this section. Modifications for particular studies are given in the following subsections. Samples consisted of the following: (a) single-crystal silicon, (b) single-crystal silicon with 1 micron of thermally-grown SiO_2, patterned to expose windows to the silicon surface, and (c) polysilicon films of 100 or 18 nm in thickness, deposited by LPCVD at 580° C on oxidized silicon wafers having 1-micron thick thermally-grown SiO_2. The samples were RCA cleaned, and immediately before loading into the sputtering system, each would receive an HF-treatment. The various HF-treatment procedures that were investigated in this work are described in the next section, having the title of Surface Preparation.

After loading into the system load-lock chamber, the samples were pumped down to less than 100 microTorr. The samples were then loaded into the main chamber. The main chamber was at a base pressure of less than 2.5×10^{-7} Torr when the sample was introduced. After pumping the main chamber to less than 1 microTorr, either cobalt or nickel was deposited using RF sputtering at 250 W from 150 mm diameter targets. Argon was used as the sputtering gas at a pressure of 9 mTorr and the targets were pre-sputtered for two minutes prior to film deposition.

The sputter rates of cobalt and nickel were 6 and 4.3 nm/min, and target to substrate distance was 150 and 100 mm respectively. After metal deposition, some samples were removed and the as-deposited metal sheet resistance was measured. For silicide samples, after extinguishing the plasma the chamber would be evacuated to less than 1 microTorr, and the sample was then moved under a quartz lamp heater for in situ annealing. After the in situ silicidation anneal, the sample was removed from the sputtering system and any unreacted metal was etched away, using a 3:1 H2O2:HCl for the cobalt samples and 3:1 H_2O_2:H_2SO_4 for the nickel samples. The sheet resistance of unpatterned samples was measured using a four-point probe setup. The sheet resistance of the bulk silicon was greater than 4 kohm/sq.

4.1.1.2 Surface Preparation Study

Various HF-dip and rinse methods were investigated to determine the effect of the rinse method and the hydrophilic/hydrophobic nature of the sample on the quality of the silicide. Single-crystal Si samples which were N_2 dried after HF dip were used as the control samples. These substrates were entirely hydrophobic after the dip. However, both oxidized silicon wafers and AMOLED glass panels are hydrophilic and the water

from the HF solution, or any rinsing solution, must be removed for vacuum integrity. In order to simulate the hydrophilic nature of glass substrates, silicon wafers with thick, thermally grown oxides were used. The experimental substrates used for this were oxidized single-crystal silicon with patterned oxide windows.

In this study the following HF-dip and rinse treatments were investigated: (a) 25:1 H_2O:HF dip (HF-dip) followed by N_2 blow dry (HF-N_2); HF-dip followed by deionized (DI) water rinse and N2 drying (HF-DI-N2); (b) HF-dip followed by isopropanol (IPA) rinse and N_2 drying (HF-IPA-N_2); and (c) HF-dip followed by DI rinse, IPA rinse, and N_2 drying (HF-DI-IPA-N_2).

After the HF treatments, 6 nm of Co or 9 nm Ni were deposited and the silicide was formed at either 700° C or 400° C for 10 minutes through an in situ annealing. This was followed by an etch to remove unreacted metal. The sheet resistances of the silicides on the various substrates with different preparation methods were then compared.

4.1.1.3 Thin Film Silicidation Study

In this study, the relationship between the deposited metal film thickness and the resulting silicide sheet resistance was explored. Additionally, the thermal and chemical stability of the silicides was quantified using sheet resistance measurements. The samples were prepared using the HF-dip, DI water rinse, IPA rinse, and nitrogen-drying treatment as described above in the surface preparation study. Cobalt was sputtered to a thickness of 3 or 6 nm and annealed at temperatures ranging from 600 to 700° C for 10 to 30 minutes, on single-crystal silicon and polysilicon samples. Nickel was sputtered to a thickness of 4 or 9 nm and annealed at temperatures ranging from 250 to 600° C, also on single-crystal silicon and polysilicon samples. Both cobalt and nickel silicide samples were formed by in situ annealing as described in the section surface preparation. After the silicidation anneal, the samples received their respective metal etches, and the sheet resistance was measured using a four-point probe. The chemical resistance of nickel silicide and cobalt silicide was examined by exposing samples to commonly-used chemicals in semiconductor processing: (a) 1:1:5 NH_4OH:H_2O_2:H_2O, (b) 1:1:5 HCl:H_2O_2:H_2O, (c) 20:1 H_2O:HF, (d) 6:1 NH4F:HF (BHF), (e) 16:1:1:2 H_3PO_4: acetic acid: HNO_3:H_2O (aluminum etch), (f) 1:50:20 HF:HNO_3:H_2O (silicon etch), and (g) 3:1 H_2O_2:H_2SO_4. The thermal stability of the nickel silicide and cobalt silicide films was explored by using furnace annealing of the samples at 600° C in an N_2 ambient over several hours, with the changes in the films being characterized using periodic sheet resistance measurements.

4.1.2 Experimental Results

4.1.2.1 Surface Preparation Study

The sheet resistance of the cobalt silicide as a function of the surface preparation method and substrate is shown in Table 4.1. The sheet resistance of nickel silicides is shown in Table 4.2. The sheet resistance is measured using four-point probe method and is the ratio of material resistivity to its thickness. It has the dimensions of ohm/sq where sq is the number of squares expressed as the ratio of length to width of resistor line. The silicides have similar sheet resistance, about 13 ohm/sq for cobalt silicide, 9 ohm/sq for nickel silicide, regardless of the surface preparation. DI-water rinsing effectively

removed liquid HF from the samples (HF-DI-N_2 and HF-DI-IPA-N_2) and did not affect the sheet resistance of the silicide films. The IPA did not degrade the surface preparation as shown by the similar sheet resistance of the IPA samples in comparison to the non-IPA samples. It is important to note that the IPA did effectively remove water from the samples, particularly the hydrophilic samples and made pump down more rapid due to the complete removal of water from the sample. Hence two conclusions can be drawn. IPA drying does not destroy the passivation of the silicon surface provided by the HF-dip. Further, DI-water rinsing does not affect the passivation provided by the HF-dip, so that the acid can be thoroughly rinsed before IPA drying. This method of preparing substrates for silicidation is applicable to large area active-matrix LCD glass panels, which are hydrophilic and consist of large areas.

Substrate	HF-N_2	HF-IPA-N_2	HF-DI-N_2	HF-DI-IPA-N_2
silicon blank	12.9	12.7	12.7	12.7
patterned oxide	12.6	11.6	12.6	11.6
polysilicon	13.5	16.6	13.0	14.6

Table 4.1 Sheet Resistance (ohm/sq) of Cobalt Silicide with Different Surface Preparation. (All silicides were formed by annealing 6 nm of cobalt at 700° C for 10 minutes)

Substrate	HF-N_2	HF-IPA-N_2	HF-DI-N_2	HF-DI-IPA-N_2
silicon blank	9.8	10.5	9.3	10.2
patterned oxide	9.8	9.3	9.3	9.3
polysilicon	10.1	10.2	9.4	9.9

Table 4.2 Sheet Resistance (ohm/sq) of Nickel Silicide with Different Surface Preparation (All silicides were formed by annealing 9 nm of nickel at 400° C for 10 minutes)

4.1.2.2 Thin Film Silicidation Study

COBALT SILICIDE

The effect of silicidation temperature on the sheet resistance of cobalt silicide formed on single-crystal and polycrystalline silicon is shown in Figure 4.1. For 10 minutes anneals, the transition temperature from a higher resistance to a lower resistance phase is 650° C, with a final-phase sheet resistance of 13 ohm/sq. Films annealed for 10 minutes at 600° C show a high sheet resistance: 240 +/- 25 ohm/sq. The low resistance phase is fully realized at 600° C when annealed for 30 minutes, when the sheet resistance is 13 ohm/sq. Thus low resistance cobalt silicides can be made using a glass compatible process.

The sheet resistance values of cobalt silicides on 100 nm polysilicon sample and on crystalline silicon substrate were identical when formed using 600 °C and 650 °C anneals, but not at 700° C. At 700° C, the sheet resistances of the films on the polysilicon samples are greater than the silicides formed on single crystal silicon. This was observed for films formed from both 3 nm and 6 nm of cobalt. It has been reported that at high temperature anneals, >950° C, the grain size of the cobalt silicide increases, leading to an increased roughness of the film with a corresponding increase in resistivity [4.1.8]. The increase in sheet resistance of the polysilicon samples when prepared at 700° C compared to those prepared at 600° C and 650° C can be explained by similar phenomena. The higher temperature silicidation anneal leads to a greater degree of agglomeration, which results in a higher measured resistivity for those samples formed on polysilicon. As this agglomeration effect is enhanced by a polycrystalline morphology [4.1.9], the cobalt silicide samples on single crystal silicon formed at 700° C do not experience a similar increase in resistance.

Cobalt silicide samples were subjected to a variety of chemical reagents to determine their stability in common etchants. As can be seen from Table 4.3, a cobalt silicide sample can be exposed to the following chemicals without degradation: the RCA clean, the Pirhanna clean of 3:1 H_2O_2:H_2SO_4, a PAN etch, and a 3:1 mix of H_2O_2:HCl. However, the film proved completely incapable of resisting any chemical mixtures involving HF. Both the silicon etchant and even a very weak 30:1 H_2O:HF solution quickly destroyed the film.

While the cobalt silicide films lacked resiliency when exposed to certain chemicals, they proved to have excellent thermal stability at 600° C. Samples formed on single-crystal silicon and then furnace annealed at 600° C in an N_2 ambient exhibited little change in their sheet resistance over the entire annealing time of three hours, as evident in Table 4.4.

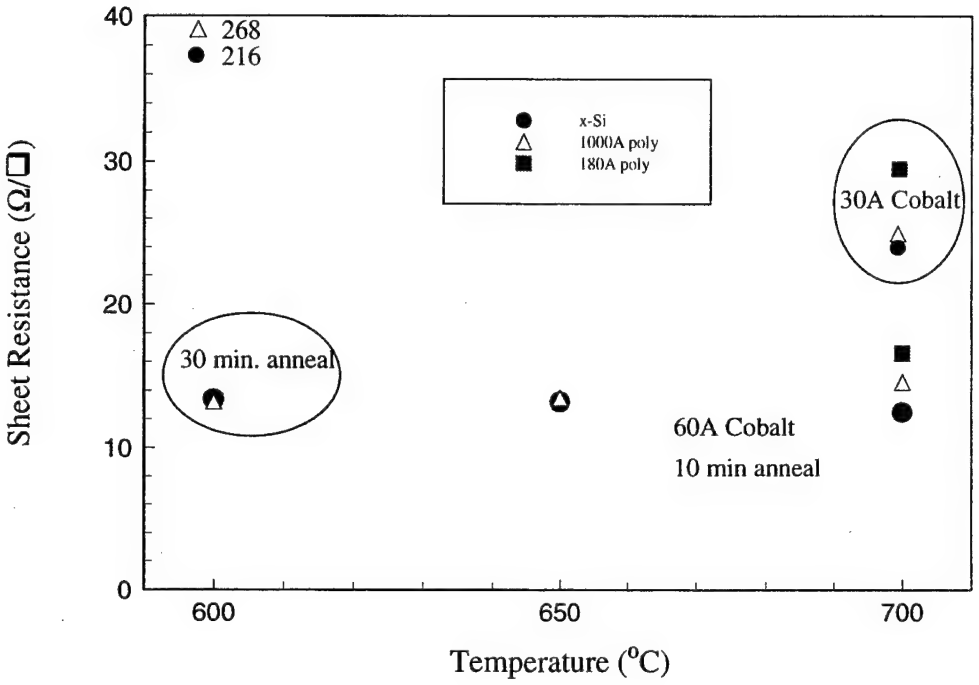


Figure 4.1 Effect of Annealing Temperature on Cobalt Silicide Sheet Resistance

Etchant Solution	Sheet Resistance (ohm/sq) of sample formed at 600° C after etch	Notes
1:1:5 $NH_4OH:H_2O_2:H_2O$	28.5	10 min
1:1:5 $HCl:H_2O_2:H_2O$	28.5	10 min
20:1 H_2O:HF	no film	2 min
30:1 H_2O:HF	96.3	30 sec
6:1 NH_4F:HF	no film	30 sec
16:1:1:2 H_3PO_4: CH_3COOH: HNO_3: H_2O	28.5	2 min, 60° C
1:50:20 $HF:HNO_3:H_2O$	no film	2 min
1:1:5:3 H_2SO_4: H_3PO_4: CH_3COOH: HNO_3	30.3	2 min
3:1 $H_2SO_4:H_2O_2$	28.5	10 min
3:1 $HCl:H_2O_2$	28.5	5 min

Table 4.3 Chemical Reagent Testing of Cobalt Silicide. Initial Sheet Resistance of samples formed at 600° C, 30 minutes = 28.5 ohm/sq

Sample	prior to anneal	1 hour	2 hours	3 hours
Nickel Silicide formed on c-Si at 400° C for 10 min from 10 nm of Ni	8.3 +/- 3%	27.4 +/- 8%	33.6 +/- 15%	40.5 +/- 15% portions of film unreadable
Nickel Silicide formed on c-Si at 600° C for 10 min from 10 nm of Ni	9.7 +/- 5%	35.0 +/- 7%	41.5 +/- 12%	48.6 +/- 25 % portions of film unreadable
Nickel Silicide formed on c-Si at 400° C for 10 min from 30 nm of Ni	2.66 +/- 2%	2.73 +/- 3%	2.85 +/- 3%	3.05 +/- 4%
Cobalt Silicide formed on c-Si at 600° C for 30 min	28.5 +/- 2%	27.2 +/- 2%	27.2 +/- 2%	26.3 +/- 3%
Nickel Silicide formed on poly-Si at 400° C for 10 min from 10 nm of Ni	10.8 +/- 6%	film unreadable		
Nickel Silicide formed on poly-Si at 600° C for 10 min from 10 nm of Ni	28.3 +/- 5%	film unreadable		
Nickel Silicide formed on poly-Si at 400° C for 10 min from 10 nm of Ni annealed in N_2	10.9 +/- 5	24.3 +/- 6%		26.5 +/- 6%
Nickel Silicide formed on poly-Si at 400° C for 10 min from 10 nm of Ni annealed in vacuum	10.9 +/- 5	22.3 +/- 6%		22.8 +/- 5%
Nickel Silicide formed on poly-Si at 400° C for 10 min from 30 nm of Ni	3.0 +/- 6%	4.53 +/- 3%	5.1 +/- 4%	5.7 +/- 5%

Table 4.4. - Effect of furnace annealing on various silicides' sheet resistances. Annealing performed at 600° C in atmosphere or as labeled. Units of sheet resistances are in ohm/sq.

NICKEL SILICIDE

Figure 4.2 shows the sheet resistance values of nickel silicides on various substrates formed by nickel sputtering, followed by a 10-minute anneal at various temperatures. The nickel silicide film exhibited a low sheet resistance in the temperature range from 400 to 500° C, with values of 8.5 +/- 0.2 ohm/sq for silicides on single-crystal silicon, and 8.0 +/- 0.2 ohm/sq for silicides on thick polysilicon. These sheet resistance values are in accord with having formed the monosilicide phase of the nickel silicide [4.1.10]. According to Pretorius, the phase of the nickel silicide formed is not a function of annealing temperature as much as it is a function of the effective concentration at the interface of the binary system [4.1.11]. Accordingly, Ni_2Si or NiSi should initially form, and once all the nickel has reacted, the $NiSi_2$ phase begins to form. Therefore, from the sheet resistance characteristic, less nickel was consumed at the silicidation temperatures of 250 and 300° C, which formed a thinner silicide with higher resistance. At 600° C the silicon-nickel reaction had proceeded far enough along for a silicon rich phase transition, as evident from the increasing sheet resistance [4.1.9].

Figure 4.3 shows the effect of thickness of the deposited nickel on the sheet resistance of the annealed silicide on different substrates. When 4 nm of nickel was used, the silicide sheet resistance was about twice that of the 9 nm nickel samples. To determine whether there was unreacted nickel on the surface after the anneal, the sheet resistance of the 4 nm and 9 nm sputtered nickel films were measured before and after etching. The measured sheet resistances were unchanged by the etch. This indicates complete consumption of the nickel film during the silicidation anneal. Thus, while the sheet resistance of the nickel silicide scales with the thickness of the reacted nickel, reducing the polysilicon film thickness results in a higher nickel silicide sheet resistance. The grain structure of polysilicon is in part a function of the film thickness, with smaller grains being associated with thinner films [4.1.12]. The increased sheet resistance of the nickel silicide on the thin (18 nm) polysilicon is attributed to the finer grain microstructure.

The chemical stability of the nickel silicide was studied for a series of chemicals used in semiconductor processing. A sample of NiSi on single-crystal silicon, with an initial sheet resistance of 9.8 ohm/sq, was exposed to the chemicals listed in Table 4.5. The ammonia-based portion of the RCA clean or the Pirhanna clean did not affect the nickel silicide. However, on certain nickel-rich silicide films formed on polycrystalline silicon, etchants containing HCl, such as the second portion of the RCA clean, were observed to destroy the silicided islands. Although nickel silicide was found to be far more resistant than cobalt silicide to HF solutions, some degradation was observed in the various HF solutions: HF-dip, BHF, and the silicon etchant. The HF and BHF solutions left a mirror-like surface when the film was only exposed to the etchant once, but multiple dips in the etchant caused some fogging of the remaining film. A cloudy surface was also observed when nickel silicide was exposed to the silicon etchant. How the HF solutions caused the degradation of the nickel silicide was a strong function of whether or not the silicide was placed in the etchant a number of times, or just exposed in a prolonged dip in the etchant solution. It seems that the HF solutions have a self limiting reaction with the nickel silicide, forming a by-product on the surface of the film that prevents further etching.

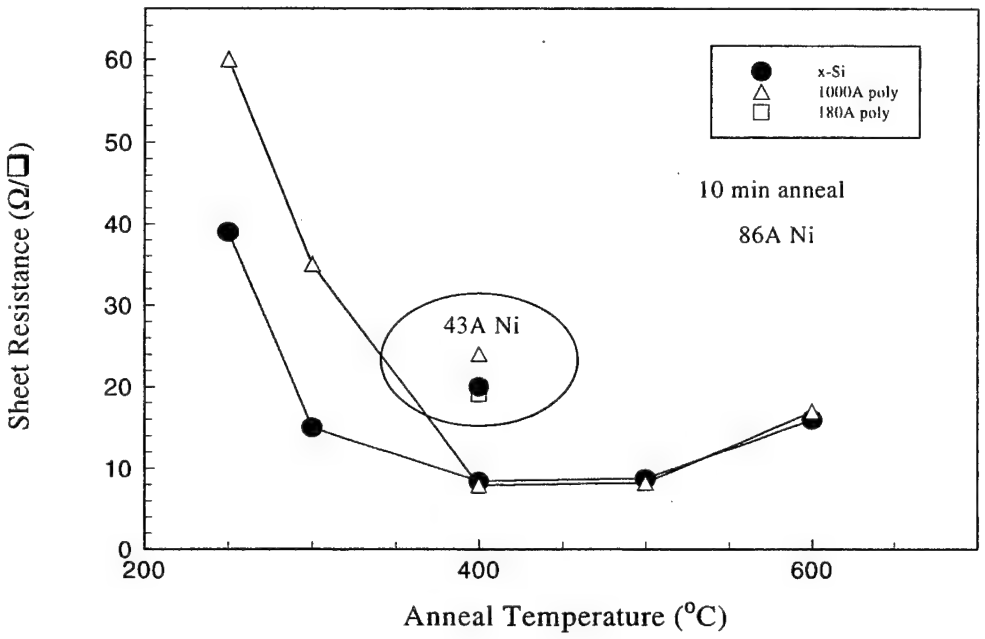


Figure 4.2 Effect of Annealing Temperature on Nickel Silicide Sheet Resistance.

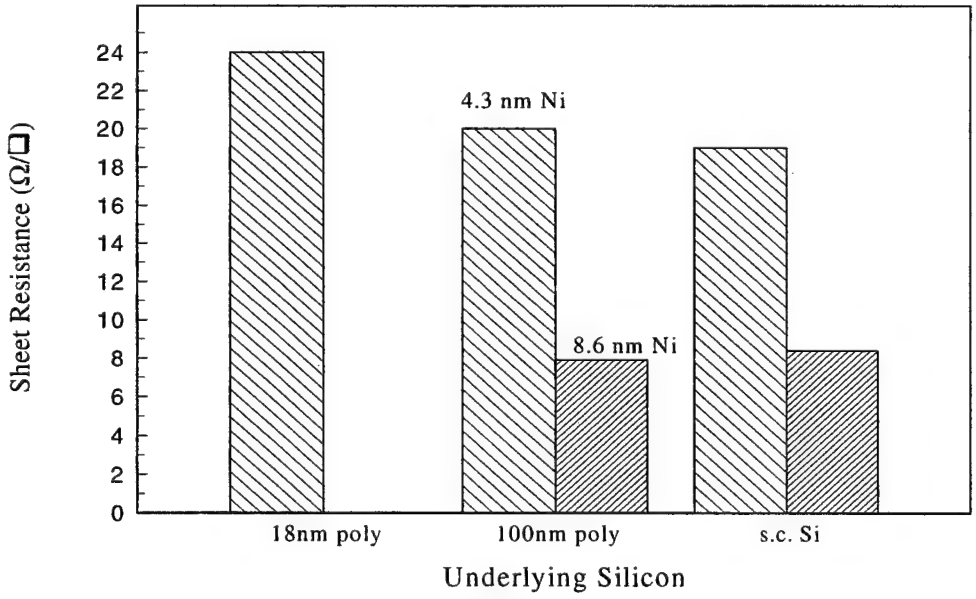


Figure 4.3 Effect of Nickel Thickness on Sheet Resistance (ohm/sq) of Nickel Silicide

Etchant Solution	Sheet Resistance (Ohm/sq) of sample formed at 400° C after etch	Sheet Resistance (ohm/sq) of sample formed at 600° C after etch	Notes
1:1:5 $NH_4OH:H_2O_2:H_2O$	9.5	11.3	10 min
1:1:5 $HCl:H_2O_2:H_2O$	9.9	11.3	10 min
20:1 H_2O:HF	13.6	14.5	2 min
	22.2	24.9	2 + 3 min
	161.7	65.7	2 + 3 + 5 min
	14.5	19.5	5 min
	16.8	18.1	10 min
6:1 NH_4F:HF	11.8	18.1	30 sec
	26.7	-	30 + 30 sec
	41.7	-	0.5 + 0.5 + 1 min
	173.0	-	0.5 + 0.5 + 1 + 2 min
	18.1	18.1	4 min
	14.5	22.7	10 min
16:1:1:2 H_3PO_4: CH_3COOH: HNO_3: H_2O	9.5	11.3	2 min, 60° C
1:50:20 $HF:HNO_3:H_2O$	no film	no film	2 min
1:1:5:3 H_2SO_4: H_3PO_4: CH_3COOH: HNO_3	11.3	11.3	2 min
3:1 $H_2SO_4:H_2O_2$	9.5	11.3	10 min
3:1 $HCl:H_2O_2$	9.5	11.3	5 min

Table 4.5 Chemical Reagent Testing of Nickel Silicide.

Initial Sheet Resistance of samples formed at 400° C, 10 minutes = 9.5 ohm/sq
Initial Sheet Resistance of samples formed at 600° C, 10 minutes = 11.3 ohm/sq

Formation of a by-product on the surface of the film was confirmed by x-ray photoelectron spectroscopy (XPS) analysis as elaborated below. Figure 4.4 indicates Ni-2p spectra obtained from the nickel silicide film after a variety of chemical treatments. The spectrum (a) in Figure 4.4 was obtained from the control specimen which was formed by thermally anneal at 400° C for 10 minutes of 10 nm of nickel. Any unreacted nickel was removed from the control specimen using a Pirhanna etch before XPS analysis. From the binding energy position of the spectrum peak (853.6 eV), it is clear that the control specimen has only NiSi at the surface. When the control specimen was dipped in buffered HF solution for a minute and then blow-dried with nitrogen without any rinsing, the resulting by-product on the surface was quantified using XPS. Ni-$2p_{3/2}$ peaks at 857.5 eV and 864.2 eV, present in the spectrum obtained from the non-rinsed

specimen i.e., spectra (c) in Figure 4.4 confirm a reaction by-product at the surface. The physical action of rinsing after etching appears to remove this protective by-product as evident from the disappearance of these two peaks from spectrum (c) in Figure 4.4, which was obtained from the rinsed specimen. Thus subsequent dips in the etchant solution cause rapid degradation of the nickel silicide sample. When the nickel silicide is attacked by buffered BF, some metallic nickel also forms which redistributes itself on the surface after rinsing. This is clear from the metallic nickel peak at 852.4 eV in spectrum (b). The small peak at 856 eV in spectrum (b) is due to nickel hydroxide formation at the surface.

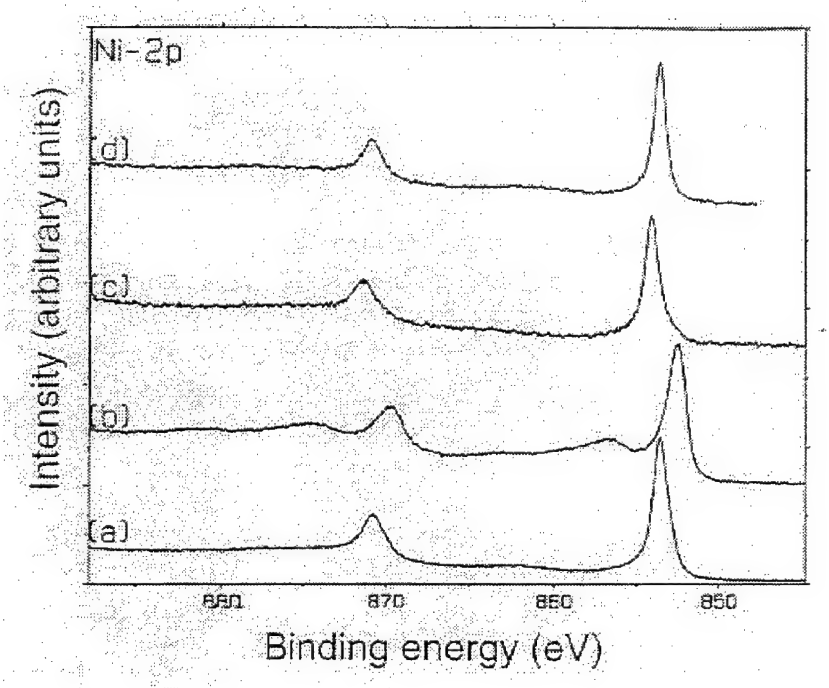


Figure 4.4 Ni-2p spectra obtained from nickel silicide on polysilicon (formed from 10 nm of Ni, silicidation anneal 400° C for 10 minutes) specimens subjected to treatment in buffered HF (6:1): (a) control specimen, no BHF treatment, (b) specimen dipped for one minute in BHF and rinsed in DI water, and (c) specimen dipped for one minute in BHF, blown dry with N_2.

The thermal stability of nickel silicide films was also studied by measuring the sheet resistance of these films periodically during an anneal at 600° C in atmosphere over several hours. What can be seen from Table 4.4 is that a nickel silicide formed on single crystal silicon from 10 nm of nickel experienced continuous degradation. By the end of the three-hour anneal, the sheet resistance of films formed at both 400° C and 600° C increased by a factor of five. The variation in the measured sheet resistance of these films also increased over the course of the annealing and after three hours of annealing it became extremely difficult to get a stable measurement from the four-point probe apparatus, with parts of the samples becoming unreadable. The films formed on polysilicon at 400° C and 600° C experienced a more severe problem, becoming unreadable by the four-point probe apparatus after a single hour of annealing.

Ni-2p spectrum obtained from a control specimen (again with 10 nm of nickel was deposited on 50 nm polysilicon and then annealed at 400° C for 10 minutes, with any unreacted nickel being subsequently removed using a Pirhanna etch) using XPS analysis, is indicated in Figure 4.5 (spectrum a). Other than the Ni-$2p_{3/2}$ and Ni-$2p_{1/2}$ peaks due to NiSi formation, no other peak is visible in the spectrum. Annealing this control specimen at 600° C decomposes the silicide at the surface into metallic nickel, nickel oxide and SiO_2. Presence of metallic nickel at the surface is evident from the peak at 852.4 eV in spectrum (b) of Figure 4.5. The nickel oxide peak is submerged below the hydroxide peak (856 eV), so oxide formation is not very evident from the Ni-2p spectrum. The surface hydroxide peak formed when the specimen was exposed to atmosphere during transfer from the annealing furnace to the XPS analysis chamber. Nickel oxide formation is indicated better in the deconvoluted O-1s spectrum (Figure 4.6) at 531.2 eV which was obtained from the same specimen. The other product of decomposition, SiO_2 is clearly visible from both O-1s (Figure 4.6) and Si-2p spectra (Figure 4.7). The difficulty in obtaining accurate measurements from the thin nickel silicide samples with the four-point probe apparatus was therefore evidently caused by oxide formation at the surface.

Decomposition of the silicide on the control specimen during annealing at 600° C can be prevented by flowing nitrogen through the furnace as Spectrum (c) in Figure 4.5 indicates. The only peaks in this spectrum are due to NiSi (like that in the control specimen). This result is confirmed by the sheet resistance measurements. Table 4.4 indicates that nickel silicide samples annealed in N_2 or vacuum did not experience the degradation in sheet resistance observed in those samples annealed in atmosphere.

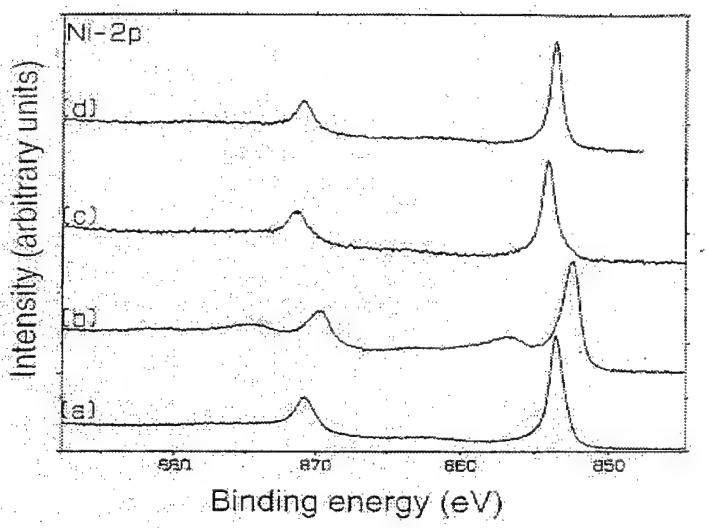


Figure 4.5 Ni-2p spectra obtained from Ni silicide on polysilicon (formed from 10 nm of Ni, silicidation anneal 400° C 10 minutes): (a) control specimen, no anneal beyond silicidation anneal, (b) annealed 600° C, one hour in atmosphere, (c) annealed 600° C, one hour in nitrogen, and (d) specimen formed from 20 nm of Ni, silicidation anneal 400° C 10 min, annealed 600° C, one hour in atmosphere.

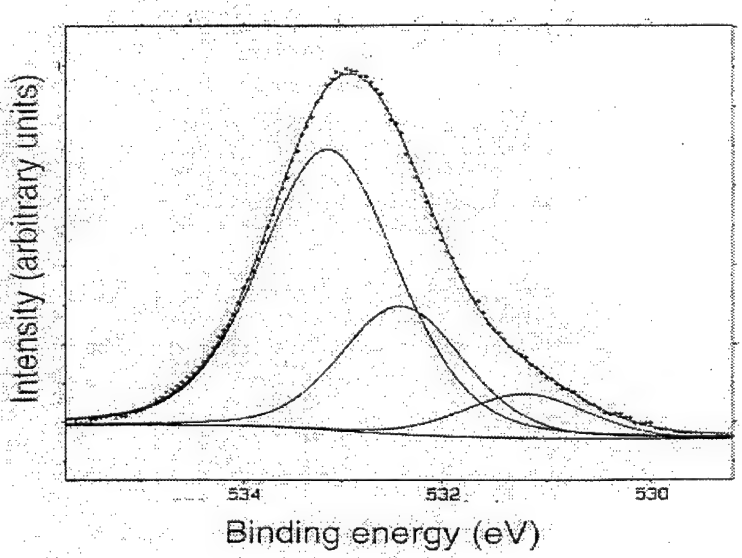


Figure 4.6 The deconvoluted O-1s spectrum obtained from Ni silicide on polysilicon shown in Figure 4.5(b) (annealed one hour, 600° C in atmosphere after silicidation anneal). The peak at 531.2 eV is attributed to nickel oxide formation, the peak at 532.4 eV due to surface hydroxide and the peak at 533.1 eV due to SiO_2 formation after decomposition of the silicide.

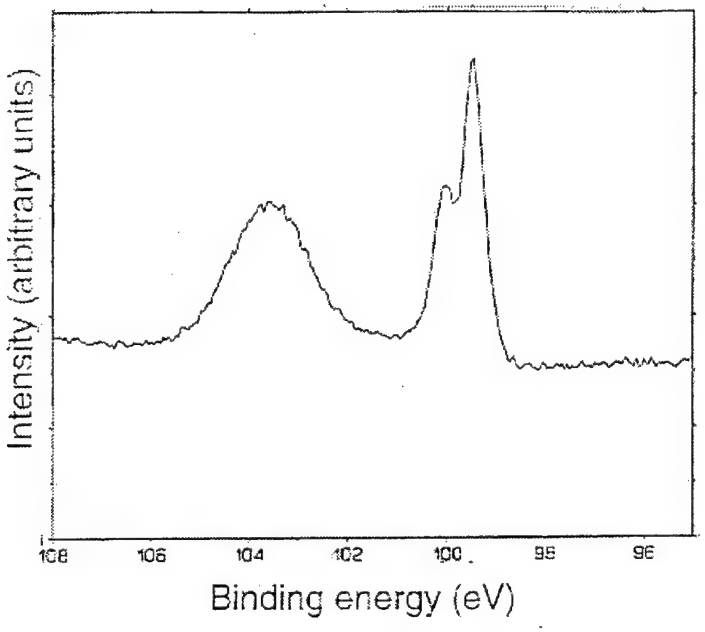


Figure 4.7 Si-2p spectrum obtained from nickel silicide specimen on polysilicon shown in Figure 4.5(b) (annealed one hour, 600 °C in atmosphere after silicidation anneal). The peak at 103.5 eV is due to SiO_2 formation after decomposition of the silicide.

The higher sheet resistance of the sample annealed in N_2 is attributed to some slight oxidation caused by the presence of some oxygen in the N_2 ambient. Thicker silicide films, formed by depositing 30 nm of nickel on either single crystal silicon or polycrystalline silicon and then annealed for 10 minutes at 400° C in the manner described previously, were also tested for thermal stability. Unlike the corresponding thin silicide films formed using 10 nm of nickel, the thicker nickel silicide on single crystal silicon demonstrated a sheet resistance, which proved to be very stable over the course of the furnace annealing in atmosphere. As depicted by Table 4.4, the thicker nickel silicide experienced only a slight increase in sheet resistance and the variation in the measured values also remained very low over the course of the annealing. The thicker nickel silicide on polysilicon had a similar response to the furnace annealing, demonstrating an early ~50% increase in sheet resistance after one hour, and then a more gradual increase in sheet resistance, with little variation in measured values. It is clear from the Ni-2p spectrum obtained from such a specimen (spectrum (d) in Figure 4.5) that the nickel silicide did not decompose, as had the thinner sample. The Ni:Si ratio in the silicide in this specimen is higher than that of the control specimen where 10 nm of nickel was used. Hence the Ni-$2p_{3/2}$ peak in spectrum (d) is at a lower binding energy than that in spectrum (a) and (c) of Figure 4.5.

4.1.3 Conclusions

Using a fabrication procedure applicable to polysilicon thin film transistors and AMLCD processing, low-resistance silicides of cobalt and nickel were fabricated on polysilicon with a thickness as thin as 18 nm with sheet resistances as low as 16 ohm/sq. Films with lower resistances were formed on thicker polysilicon samples: 8 ohm/sq NiSi, and 14.6 ohm/sq $CoSi_2$. The sheet resistance of cobalt silicide is slightly dependent on the structure of the silicon underlayer. Low-resistance cobalt silicides were formed by annealing for 30 minutes at 600° C or 10 minutes at 650° C, while low-resistance nickel silicides were formed by annealing for 10 minutes at 400° C.

A reliable process for surface preparation prior to silicide formation has been developed. IPA rinsing that follows the HF dip and H_2O rinsing preserves the passivation of a HF-cleaned silicon surface while dehydrating hydrophilic surfaces. This in turn enables an easier and more complete evacuation when the sample is loaded into the vacuum. IPA rinsing can be used in both silicon integrated circuit and glass substrate AMLCD fabrication.

Nickel silicide has been shown to be chemically suited for semiconductor processing, though care must be employed to avoid multiple exposures to wet HF solutions, which cause some degradation. Cobalt silicide films were non-resistant to aqueous HF and were quickly destroyed when exposed for even short periods of time. However, cobalt silicide did show itself to be more thermally stable than the nickel silicide, remaining unchanged for the most part during a 600° C furnace anneal in atmosphere. In contrast, nickel silicide films saw a severe degradation in their sheet resistance as a result of some form of oxidation during the furnace anneal when the silicide in question was formed using a thin, 10 nm layer of nickel. Thicker nickel silicides formed from 30 nm of nickel, or thin films annealed in N_2 or vacuum did not experience this type of degradation and oxidation did not appear as a problem in these films.

4.2 Elimination of Hillock Formation in Al Interconnects Using Ni, Co Interlayers

Aluminum alloy interconnections are commonly used in the microelectronic industry. In integrated circuit (IC) manufacturing, aluminum/aluminum alloys are the primary metallization materials because their low resistance leads to a decreased time delay and lower power consumption. In AMLCD fabrication, aluminum has started to replace refractory metals as the material of choice for both data and scan lines because increasing display sizes have mandated a decrease in the resistance of metal lines. Aluminum-based metallization has also been adopted in the development of polysilicon thin film transistor based AMOLED displays, which operate on current based driving schemes [4.2.1].

In both microelectronic interconnect technology with multilevel metallization layers and in display fabrication, hillock formation leads to interlevel metal shorts [4.2.2, 4.2.3], which present a reliability concern. Interconnects made of Al-Cu, Al-Si, and Al-Cu-Si alloys, although better than unalloyed aluminum interconnects [4.2.4] in certain composition ranges in their hillocks reduction and junction spiking elimination capabilities, do not totally eliminate hillock formation [4.2.5, 4.2.6]. Additions of Fe, Ni, Co, Ti, Ta, Zr, Hf, Cr, Mo, Y, and Nd (Reference 4.2.7-14) to Al, Al-Cu, Al-Si, and Al-Cu-Si sputtering targets to yield hillock-free films have also been reported. Even though the resistance to hillock formation was shown to improve in some cases over narrow

alloying additions and temperature ranges, this often came with the cost of increasing electrical resistivity or thermal and mechanical instability of the films. Electrical resistivity increased primarily because of formation of grain boundary precipitates, which were distributed homogeneously in the film. Gardner et al. [4.2.15] had proposed that bilayer Ti/Al-1%Cu metallization stacks were better than single layer Al-1%Si films with metal additives distributed homogeneously for reducing hillocks in multilevel interconnects.

The bilayer approach could also offer other advantages such as lowering electrical resistivity compared to films where elements were distributed uniformly [4.2.15]. In active-matrix-display fabrication processes, Al alloys do not form good ohmic contact with ITO, which is used as the transparent electrode in an AMLCD or AMOLED structure, so an ohmic contact forming an intermediate layer between ITO and Al alloy is also necessary to obtain better device characteristics. This is of particular importance for the current driven AMOLED display pixels. Even though Ti can form an ohmic contact between Al and ITO, a Ti layer is prone to guttering affects during the hydrogenation step necessary in the passivation of polysilicon TFTs used in high resolution, small area display applications. While titanium based multilevel aluminum metallurgy (such as TiN/Ti/Al-Cu/TiN) is commonly used in very large scale integrated (VLSI) processing, the less stringent design rules in display fabrication call for a simpler metallization scheme that avoid the complexities of current VLSI multilevel metallization processes such as the chemical mechanical polishing. Information regarding whether TiN forms an ohmic contact with ITO could not be readily obtained from the literature.

It was demonstrated earlier that Co and Ni layers form good ohmic contacts with ITO, hence both these elements have potentials for use in AMLCD metallization processes [4.2.16]. The case for incorporating cobalt and nickel deposition steps during display manufacturing is also strengthened by the fact that both these elements are easy to sputter; unlike a material like TiN which involves reactive sputtering or sputtering from composite targets where stoichiometries are harder to maintain. Furthermore cobalt and nickel form silicides at temperatures suitable for making active matrix displays on low cost glass substrates. These silicides are useful in reducing parasitic series resistance on the source, drain and gate regions of the TFTs used in display arrays. However, before metallization schemes involving Ni or Co can be devised, hillock formation studies in bilayer aluminum alloy metallization stacks with these elemental layers need to be carried out. This has been done in the present work.

4.2.1 Preparation Conditions

Test samples were prepared on 100 mm oxidized silicon wafers of (100) orientation since this substrate is of comparable nature to interlevel passivation oxide on which aluminum lines are deposited during display fabrication. Three different materials, nickel, cobalt, and titanium (for comparison) were used in conjunction with an Al-1%Cu film to try to minimize hillock formation. A nickel, cobalt, or titanium film was deposited either before or after the Al-1%Cu film deposition. Additionally, some samples were prepared only with sputtered Al-1%Cu or Al-1%Si film as a control. The Al alloys were DC magnetron sputtered in an argon ambient of 4 mTorr at 500 W of power from a 150 mm diameter target. Cobalt, titanium, and nickel films were deposited in an argon ambient of 9 mTorr using RF sputtering at 250 W of power from their

respective 150 mm diameter target. All aluminum films were deposited to a thickness of 200 nm, while the cobalt, nickel, and titanium films were each 50 nm in thickness. Additionally, some samples were made using a 10 nm thick nickel layer and 240 nm thick aluminum layer. Various heat treatments during and immediately after deposition were also used. For some samples a heated substrate was used in deposition, since a heated substrate can be valuable for step coverage considerations [4.2.17]. In such examples, the sample was heated at 500° C for 10 minutes prior to the first metal deposition (titanium, nickel, or cobalt). The first metal film was then deposited, followed by a second in situ heat treatment, at 500° C for five minutes. This was followed by Al-1%Cu film deposition. This particular heat treatment will be referred to as "pre heat" treatment.

Due to adhesion considerations, it was often necessary to anneal the as-deposited double layer films in situ for a short period in order to make patterning possible in cases where a heat treatment prior to deposition (pre-heat) was not used. This *in-situ* anneal was performed at 500° C for five minutes. This heat treatment will be referred to as post-heat treatment. Some double layer films were not heated during deposition and these films will henceforth be referred to as unheated films. All pre-heated, post-heated, and unheated films were finally annealed at 400° C for 30 minutes in a H_2-N_2 (10%-90%) ambient. A complete list of specimens prepared for this work is provided in Table 4.6. The temperature for the various heat treatments was chosen to test hillock formation resistance of metallization schemes at the upward limit of the thermal budget appropriate for a polysilicon TFT display array process.

4.2.2 Experimental Characterization

Hillocks in metallization stacks were then analyzed using scanning electron microscopy (SEM) and atomic force microscopy (AFM). To estimate the density of hillocks, SEM micrographs of the metallization stack surface were obtained at magnifications of 2500X from random regions of the same sample. Hillock sizes smaller than 0.05 microns are not included in density calculations. The diameters of hillocks were measured from SEM pictures and heights were obtained from AFM profiles. In almost all metallization stacks which were examined and where hillocks were present, hemispherical hillocks were observed. The only exception were hillocks in the single layer Al-1%Si film specimen which was prepared for comparative purposes. Hillock sizes measured by SEM and AFM corroborated each other very well within a factor of two. In later sections when we discuss hillock size we will be referring to hillock diameters, which were obtained from SEM analysis. Reaction products in metallization stacks were also examined using glancing angle x-ray diffraction (GA-XRD) as well as coupled scan XRD. Glancing angle scans reveal reaction products present at the metallization stack surface while the coupled scan XRD provides information from the bulk of the thin film. Film resistivity was measured using conventional four-point probe measurement at room temperature.

4.2.2.1 SEM and AFM Results

4.2.2.1.1 Single-Layer AL-1%Cu and Al-1%Si Films

The microstructures of an Al-1Cu% film which were not subjected to any heat-treatment during film sputter deposition but furnace annealed later at 400° C for 30 minutes in a H_2-N_2 (10%-90%) ambient are shown in Figure 4.8(a). The pre-heated Al-1%Cu film microstructure is shown in Figure 1(b) and an atomic force micrograph of the surface of the pre-heated Al-1%Cu film is in Figure. 4.8(c). From Figures, 4.8(a) and 4.8(b), it is clear that the topography of the pre-heated Al-1%Cu film in the non-hillock regions is rougher than that of the unheated film, however the hillock density is lower. The hillocks also have a more rounded appearance in the pre-heated film. Hillock size distribution data obtained from this and other films are summarized in Table 4.7. Table 4.7 also indicates that the hillocks in the single layer unheated Al-1%Si films were significantly larger than those observed in the unheated Al-1%Cu films, hence subsequent bilayer structures were made using only Al-1%Cu and transition metal films.

4.2.2.1.2 Ni/Al-1%Cu bilayer films

The microstructure of Ni/Al-1%Cu bilayer films, where the nickel layer is 50 nm thick, is presented in Figures 4.9(a-c). Neither the pre-heated (Figure 4.9(a)) nor the post heated (Figure 4.9(b)) film show any surface hillocks when nickel is at the bottom. The grain size of the pre-heated film is bigger than the post heated one. Similarly, no hillocks were observed even in the post-heated double layer metallization stack with nickel at the top (Figure 4.9(c)). Atomic force micrographs of Ni/Al-1%Cu bilayer films with 50 nm and 10 nm of post heated nickel on top are indicated in Figures 4.10(a) and 4.10(b), respectively. Hillocks are not visible on the surface of either of the bilayer films; the surface of the bilayer film with 10 nm of post heated nickel on top is, however, smoother. To the best of our knowledge, this is the first experimental demonstration of a hillock free aluminum metallization using Ni/ Al alloy bilayer metallization stacks.

Specimen	Deposition Heat treatment	Pre-heat Temp	Post-heat Temp	PMA treatment
Al-1%Si	(unheated)	-	-	400° C, 0.5hr, (H_2+N_2)
Al-1%Cu	(unheated)	-	-	400° C, 0.5hr, (H_2+N_2)
Al-1%Cu	(pre-heated)	500° C	-	400° C, 0.5hr, (H_2+N_2)
Al-1%Cu/Ni	(post-heated)	-	500 °C	400° C, 0.5hr, (H_2+N_2)
Ni/Al-1%Cu	(pre-heated)	500° C	-	400° C, 0.5hr, (H_2+N_2)
Ni/Al-1%Cu	(post-heated)	-	500 °C	400° C, 0.5hr, (H_2+N_2)
Co/Al-1%Cu	(pre-heated)	500° C	-	400° C, 0.5hr, (H_2+N_2)
Co/Al-1%Cu	(post-heated)	-	500 °C	400° C, 0.5hr, (H_2+N_2)
Al-1%Cu/Ti	(unheated)	-	-	400° C, 0.5hr, (H_2+N_2)
Ti/ Al-1%Cu	(unheated)	-	-	400° C, 0.5hr, (H_2+N_2)
Ti/ Al-1%Cu	(pre-heated)	500° C	-	400° C, 0.5hr, (H_2+N_2)

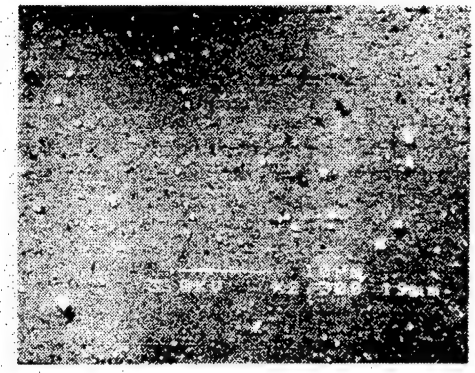
Table 4.6 List of specimens prepared

4.2.2.1.3 Case With Extra Layer Of Cobalt

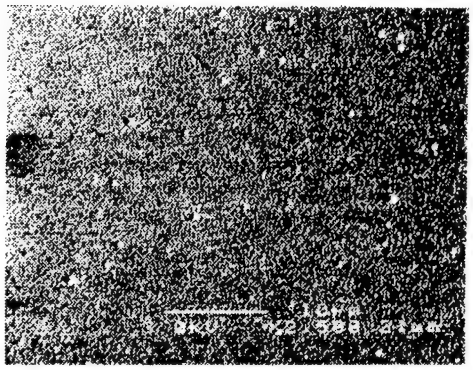
Hillocks were eliminated in the Co/Al-1%Cu bilayer film with 50 nm of preheated cobalt at the bottom as is evident from the scanning and atomic force micrographs presented in Figures. 4.11(a) and 4.2.4(b) respectively. This again is to our knowledge the first experimental demonstration of hillock free aluminum metallization using a cobalt-aluminum alloy bilayer. The grain size of this film is much smaller in the Co/Al-1%Cu bilayer film than in the Ni/Al-1%Cu bilayer film with nickel at the bottom, which was preheated at the same temperature. The post-heated film has a very high density of extremely small hillocks. The average size and density of hillocks in this bilayer film are indicated in Table 4.7. The surface topography of the post-heated film in non-hillock regions is very smooth. It is difficult to pattern films with Co on top of Al using wet etching techniques because of high lateral etching of cobalt in the aluminum wet etchant. Since the applicability of such a metallization structure was ruled out before hand, no specimens with Co on top were prepared.

4.2.2.1.4 Case with Extra Layer of Ti

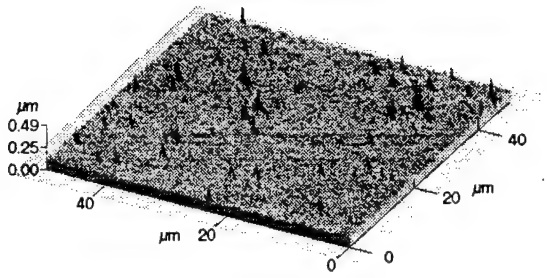
Only the unheated bilayer film with Ti at the top was hillock free. Hillocks were observed in the other unheated and preheated films. Unlike nickel and cobalt, titanium can be patterned even if the films are not heated during deposition. Hence there was no need for making post-heated films.



(a)

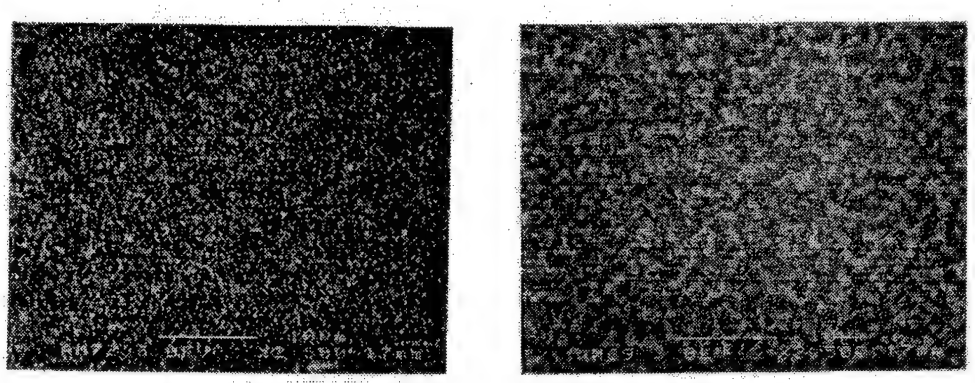


(b)

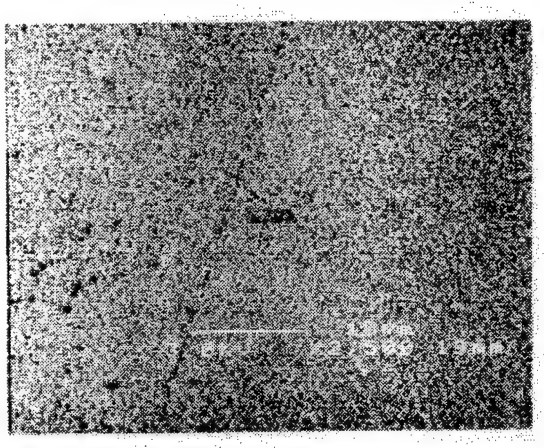


(c)

Figure 4.8 Scanning electron micrographs of the surface topography of (a) unheated Al-1%Cu film and (b) preheated Al-1%Cu film. Atomic force micrograph of (c) preheated Al-1%Cu film. Each specimen was furnace annealed at 400° C for 30 minutes in a H_2-N_2 (10%-90%) ambient.

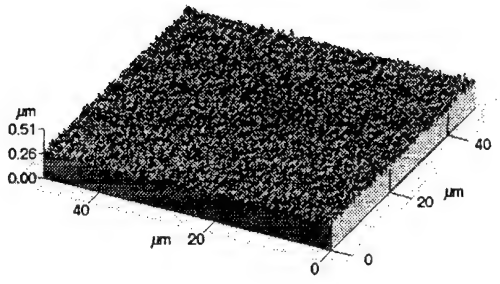


(a) (b)

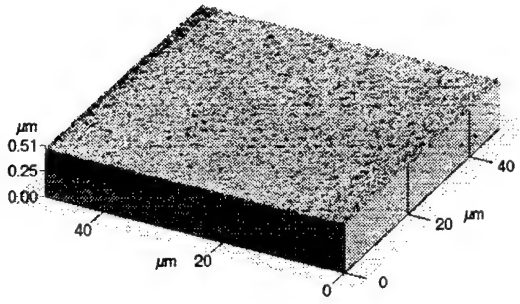


(c)

Figure 4.9 Scanning electron micrographs of Al-1%Cu film with (a) 50 nm of pre-heated nickel film at bottom, (b) 50 nm of post-heated nickel film at bottom, and (c) 50 nm of post-heated nickel film on top



(a)

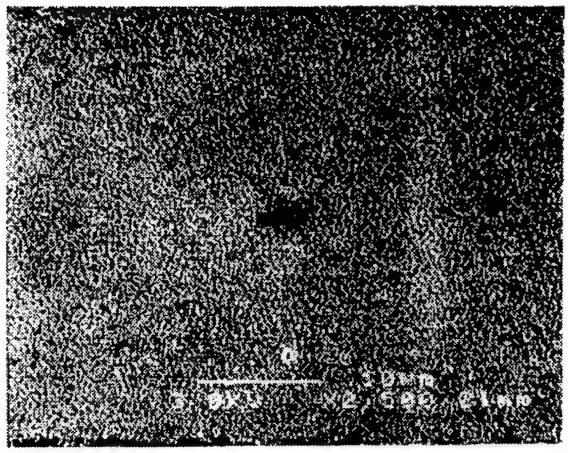


(b)

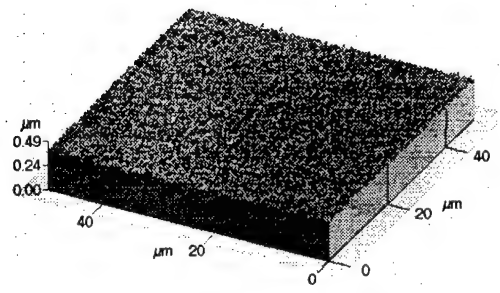
Figure 4.10 Atomic force micrographs of Al-1%Cu film with (a) 50 nm of post-heated nickel film on top and (b) 10 nm of post-heated nickel film on top

Specimen	Comments	Max hillock size (μm)	Min hillock size (μm)	Avg. hillock size (μm)		Hillock density (#/Sq. cm)	Hillock density (>0.5 μm)
	Method	SEM	SEM	SEM	AFM	SEM	SEM
Al-1%Si (unheated)		4.0	0.38	1.11	2.03	4×10^5	2×10^5
Al-1%Cu (unheated)		1.15	0.19	0.42	0.42	1.7×10^7	3.4×10^6
Al-1%Cu (preheat)		0.96	0.58	0.73	0.32	7×10^4	7×10^4
Al-1%Cu / Ni (post-heat)	No hillock						
Ni / Al-1%Cu (preheat)	No hillock						
Ni / Al-1%Cu (post-heat)	No hillock						
Co / Al-1%Cu (preheat)	No hillock						
Co / Al-1%Cu (post-heat)		0.23	0.11	0.12	0.05	3.5×10^7	-
Al-1%Cu / Ti (unheated)	No hillock						
Ti / Al-1%Cu (unheated)		0.19	0.038	0.11	0.05	1×10^6	-
Ti / Al-1%Cu (preheat)		0.77	0.19	0.58	0.26	2×10^6	2×10^6

Table 4.7 Hillock size distributions in films based on SEM observations



(a)



(b)

Figure 4.11 (a) Scanning electron micrograph of Al-1%Cu film with 50 nm of preheated cobalt film at the bottom and (b) atomic force micrograph of Al-1%Cu film with 50 nm of preheated cobalt film at the bottom

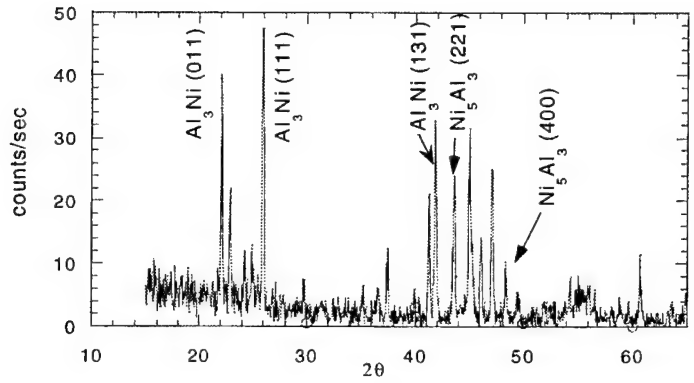
4.2.2.2 X-ray Diffraction

XRD data obtained from Ni/Al-1%Cu, Co/Al-1%Cu and Ti/Al-1%Cu bilayer metallization structures which were pre-heated at 500° C with a layer of nickel, cobalt or titanium at the bottom are indicated in Figures 4.12(a), (b), and (c) respectively. The Ni/Al-1%Cu film indicated $NiAl_3$ and very small amounts of Ni_5Al_3 formation. Even though no Al metal peak was detected in the glancing-angle scan, weak peaks of remaining Al metal were visible in the coupled scan. GA-XRD of the pre-heated Co/Al-

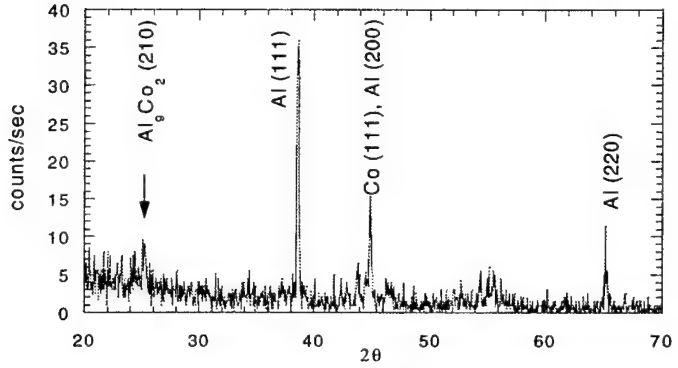
1%Cu film indicates remaining Al metal peaks and Co_2Al_9 formation. From Figure 4.12(c) it is clear that reaction products in detectable amounts did not form in the pre-heated Ti/Al-1%Cu film. Only highly textured Ti and Al peaks are visible.

4.2.2.3 Resistivity Measurements

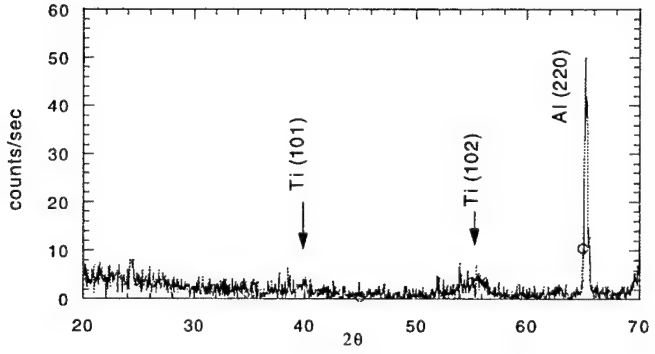
The results of resistivity measurements are summarized in Table 4.8. They indicate that an additional layer of nickel increases the resistivity of the composite metallization structure significantly, much more than cobalt or titanium. This increase can be modulated, however, by altering the ratio of nickel to Al-1%Cu. In Ti/Al-1%Cu bilayer films, the bilayer film resistivity is just slightly higher than that of the pre heated single layer Al-1%Cu film. It should be noted that the single layer pre heated Al-1%Cu film has a lower resistivity than the "unheated" film of the same composition.



(a)



(b)



(c)

Figure 4.12 XRD patterns of Al-1%Cu film with 50 nm of (a) preheated Ni at bottom, (b) preheated Co at bottom, and (c) pre-heated Ti at bottom

Specimen	Al-alloy thickness (nm)	Transition metal thickness (nm)	Resistivity (μΩ-cm)
Al-1%Si (unheated)	250	-	4.05
Al-1%Cu (unheated)	250	-	10.74
Al-1%Cu (preheat)	250	-	3.62
Al-1%Cu / Ni (post-heat)	200	50	23.08
Ni / Al-1%Cu (preheat)	200	50	21.18
Ni / Al-1%Cu (post-heat)	200	50	26.30
Al-1%Cu / Ni (post-heat)	240	10	4.3
Ni / Al-1%Cu (preheat)	240	10	4.5
Co / Al-1%Cu (preheat)	200	50	8.30
Co / Al-1%Cu (post-heat)	200	50	13.16
Al-1%Cu / Ti (unheated)	200	50	5.35
Ti / Al-1%Cu (unheat)	200	50	4.53
Ti / Al-1%Cu (preheat)	200	50	3.94

Table 4.8 Resistivity data

Material	ρ (μΩ-cm)	α ($^{o}C^{-1}$) x 10^{-6}	Ultimate tensile stress (MPa)	E (GPa)	Brinell Hardness Number	Poisson's ratio	Melting point (^{o}C)
Al	2.67	23.5	121	70.6	17	0.345	660.1
Al-1%Si			69		19		
Al-1%Cu			227		60		
Ni	6.9	13.3	482				1455
Co	6.34	12.5	230			0.361	1492
Ti	54	8.9		120.2			1667
$NiAl_3$							
Co_9Al_2							
$TiAl_3$	17-22						
Al_2Cu	5-6						
Si		3.3					1412

Table 4.9 List of physical constants of materials

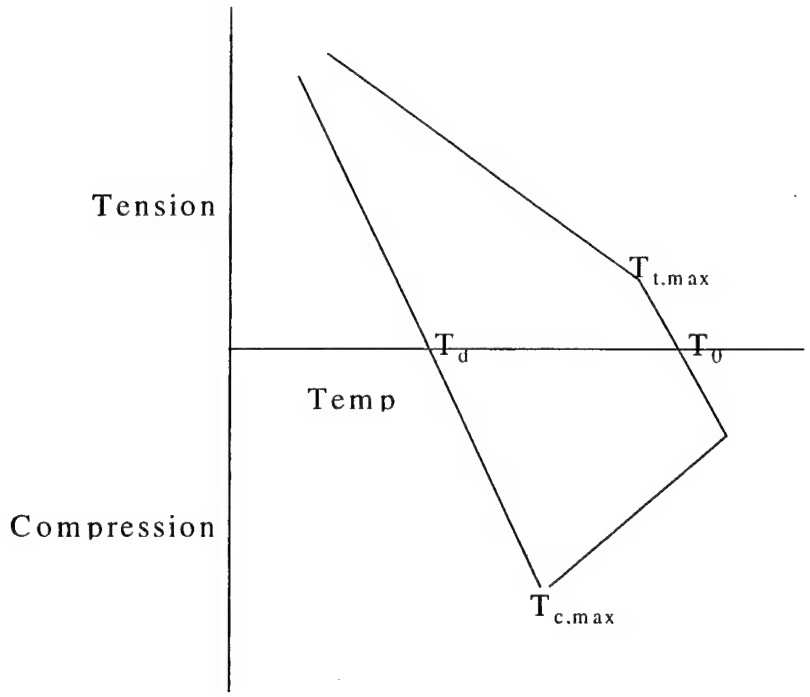


Figure 4.13 Typical stress-temperature behavior

4.2.3 Discussion of Experimental Results

4.2.3.1 Hillock Formation

Table 4.9 provides a list of physical constants of materials, which are important to understanding hillock formation mechanism in Al-alloy thin films. From Table 4.9 it is clear that the thermal expansion coefficient of unalloyed aluminum is significantly higher than that of the silicon substrate. Hence when aluminum films are deposited on silicon substrates, which are then heated, and/or cooled, compressive/tensile stress build-ups occur in the film. The stress situation in the film can be understood better by examining Figure 4.13, where T_r is room temperature, T_{dep} is the temperature of the aluminum alloy film deposition, T_o is the temperature other than T_{dep} at which the film is stress free and $T_{c,\,max}$ and $T_{t,max}$ are the temperatures at which maximum compressive and tensile stresses occur in the film [4.2.18]. T_{dep} for preheated films in our study is 500° C. When T_{dep} = 500° C, the films were annealed at a lower temperature (400° C) than T_{dep}; the stresses in these films were tensile. The post-heated and unheated films were annealed at temperatures higher than T_{dep}; therefore these films fell into the compressive stress regime of the stress-temperature curve during the post-heat treatment and annealing, respectively. The stress relaxation in the post-heated and unheated metallization structures was therefore through a compressive stress relaxation process.

The magnitude of the thermal stress caused due to differences in thermal expansion coefficients of the silicon substrate and metal layers is

$$\Phi_f = -\{E / (1-<)\}(\forall_f-\forall_s))T \qquad (4.2.1)$$

where [E / (1-<)] is the biaxial module of elasticity of the film and $\forall_f$ and $\forall_s$ are the thermal expansion coefficients of the film and substrate respectively. The stress has to be accommodated in the film through relaxation processes. A film on a substrate when subjected to a biaxial stress does not relax uniformly. There are local areas where the relaxation is larger. Once such localized differential relaxation occurs, a potential gradient is generated between the relatively relaxed grain and the surrounding film. Chaudhury [4.2.19] has proposed that this causes mass flow along the interface between the films that results in a relaxed area growing out from the base as a hillock. The hillock is pushed out from the base and slides along grain boundaries connecting it to the rest of the film. Chaudhury proposed that another stress relieving mechanism, diffusional creep (Nabarro-Herring creep [4.2.20]) can also operate concurrently. Diffusion creep is caused by mass transport through lattice or grain boundary diffusion and normally leads to relaxation rather than deformation in thin films. However, if the relaxation is homogeneous (i.e., localized), it induces hillock formation or void growth. Constitutive relations between stress and strain rate for diffusion creep has been provided by Ashby [4.2.21]

$$d,/dt = (14\Phi\Sigma/kT)\,(1/d^2)D_v\,\{1 + (B*/d)(D_B/D_V)\} \qquad (4.2.2)$$

where Σ is the atomic volume, d the grain size, D_v the bulk self diffusion coefficient of Al in the film, D_B the grain boundary diffusion coefficient, * the effective, : the shear modulus, and b the Burger's vector. When bulk diffusion controls the strain rate in diffusion creep, the first term of the diffusion creep equation is important; this creep is called Nabarro-Herring creep. When grain boundary diffusion controls the strain rate, the second term in the diffusion creep equation is the controlling one; this creep is called Coble creep. From the equation it is clear that if diffusion creep contributes to hillock formation, reduction of hillocks can be achieved through a decrease in diffusion coefficients (can be achieved through alloying) and by increasing the grain size of the film.

Interface reactions, grain growth, and other phase transformation processes in thin films can also affect the stress state of films and play a role in determining whether hillocks will form to relieve stresses. Very often hillock growth is caused by an interplay of all the factors mentioned, so while examining the results presented in the previous section all the mentioned factors have to be taken into consideration.

4.2.3.1.1 Single Layer Al-1%Cu and Al-1%Si Films

When no additional transition metal layer was used hillocks were seen in the unheated Al-Si and Al-Cu films. Compressive stress relaxation occurred in both films during heating and cooling of the annealing process. Al_2Cu phase segregation along grain boundaries and at triple points in the unheated Al-1%Cu film may have provided hillock nucleation sites during hillock formation through diffusional creep. Pre-heating the Al-1%Cu film increased the grain size and caused precipitate coarsening. Precipitate coarsening led to an increase in the size of precipitates along with a decrease in their density and a consequent decrease in the number of hillock nucleation sites. Thus the hillocks in the pre-heated Al-1%Cu film are fewer in number but bigger in size than hillocks in the unheated film. Dislocation glide motion and grain boundary sliding occur

more easily in Al-Si alloys in comparison to Al-Cu alloys, hence Al-Si alloys are more ductile and flow more easily [4.2.22]. This led to a greater reflow of material in the "unheated" Al-Si film and the creation of huge hill and crater structures.

4.2.3.1.2 Ni/Al-1%Cu bilayer films

All the Ni/Al-1%CU films, which were examined, were hillock irrespective of the stress state (compressive or tensile) in the film and the initial thickness of the nickel layer. GA-XRD of the double layer film, which was pre-heated at 500° C, revealed that the extra nickel layer was consumed totally during $NiAl_3$ formation. Since unreacted Al was not detected using GA-XRD and very weak Al-peaks were detected using coupled scans, it is clear that a very small amount of unreacted Al is present in the annealed metallized structure. The microstructure indicated in Figure 4.9(a) is due to $NiAl_3$ grains. Formation of $NiAl_3$ is accompanied by an increase in volume of the film because the atomic volume of the product $NiAl_3$ is greater than that of the reactants, Ni and Al-1%Cu. Volume changes during interfacial reactions have been calculated using the model proposed by Gardner et al [4.2.23]. The positive volume change in the entire film can contribute to reduction of tensile thermal stress, which in turn decreases the driving force to form hillocks. Formation of $NiAl_3$ at the interface with the silicon substrate also slows down diffusion of aluminum atoms at that interface which is beneficial to hillock reduction.

When the biaxial thermal stress during annealing is compressive, formation of $NiAl_3$ will increase the magnitude of the compressive stress. Even then, no hillocks were observed in any of the metallized structures (Figure 4.9(b), Figure 4.9(c)). Mechanical properties like hardness, yield strength, etc. of nickel aluminum intermetallics are significantly better than that of aluminum [4.2.24] and the rate of diffusion of Al atoms through $NiAl_3$ is lower. Hillock nucleation sites, which are caused by local stress relief mechanisms like grain boundary sliding, dislocation slips, etc. are possibly reduced because of the better mechanical properties of $NiAl_3$. Even if some hillock nucleation sites form, hillocks will be prevented from growing. In Ni/Al-1%Cu films, where nickel was deposited at the top, the harder layer of $NiAl_3$ will act as a cap to suppress hillock formation; with deposited nickel at the bottom, hillock formation will be suppressed by slow diffusion of aluminum atoms through the $NiAl_3$/substrate interface.

4.2.3.1.3 Case With an Extra Layer of Cobalt

Hillocks are absent in the pre-heated Co/Al-1%Cu bilayer film with the layer of Co at the bottom (Figure 4.11a). Formation of the compound Co_2Al_9 was detected by GA-XRD (Figure 4.12(b)) in this metallization structure along with unreacted Al. Co was totally consumed during reactions. As unreacted Al is detected just by using GA-XRD analysis without having to do a coupled scan, it is clear that there is more unreacted Al in this metallization stack than in the Ni/Al-1%Cu bilayer film which was also subjected to the same heat treatment (Figure 4.12(a)). It is likely that formation of this compound prevented fast diffusion of Al atoms through the Co_2Al_9/substrate interface and prevented hillock growth. A high density of very small hillocks were visible in the post-heated bilayer metallized film with Co at the bottom (Figure 4.11(b)) which suggests that in-spite of significant nucleation of hillock, very little growth occurred in this film. In the post-heated metallization structure, the biaxial stress is compressive. Volume change of

the film (similar to that discussed in the previous section) during Co_2Al_9 formation increased the level of compressive stress, possibly contributing to localized stress relief mechanisms in the film by generating dislocation slip, grain boundary sliding, etc. which in turn contributed to hillock nucleation. This situation is quite unlike that in the pre-heated film where the tensile stress was reduced through compound formation. Slow diffusion of Al atoms at the substrate interface compared to that in the single layer Al-1%Cu film prevents significant growth of the nucleated hillocks in the post-heated film.

4.2.3.1.4 Ti/Al-1%Cu Bilayer Films

GA-XRD of the pre-heated film with Ti at the bottom indicates no intermetallic compound formation (Figure 4.12(c)), but peak shifts indicate that the Ti layer is considerably strained. The grain size of metal layers in this film (Figure 4.12(c)) is also smaller than that of the reaction product, $NiAl_3$ layer which formed when Ni was used as the extra layer (Figure 4.9(a)). Hence, greater mass atomic transport through grain boundaries and the interface must have caused some hillock growth in the Ti/Al-1%Cu metallization structure. Hillock free metallization in Ti/Al-1%Cu bilayer films with Ti at the top could only be obtained when there was no heating during the deposition, i.e., the unheated film (Figure 4.12(b)). In this case, the deposited titanium probably acted as a hard cap suppressing hillock growth. However hillock formation could not be suppressed when the layer structure was reversed in the unheated film, i.e., when titanium was at the bottom (Figure 4.12(b)). The use of titanium for hillock suppression therefore appears to be less robust than the process using Ni in the bilayer. While a nickel layer was capable of preventing hillock formation when deposited either below or above the Al-1%Cu layer, the titanium layer only worked when above the Al-1%Cu layer. Additionally, the Ti/Al-1%Cu bilayer films appear to be sensitive to heat treatments with regard to hillock formation which is demonstrated by the fact that the preheated sample experienced larger hillock growth than the unheated sample.

4.2.3.2 Electrical Resistivity

In a 4-point probe resistivity measurement set-up for bilayer metallization structures, the resistances of the Al-1%Cu and the transition metal are set up in parallel. If Δ, Δ_1, Δ_2, and Δ_3 are the resistivities of the bilayer film, the Al-1%Cu layer, the transition metal layer and the interfacial reaction product layer, then it can be easily deduced that

$$\Delta = (1+ x + y)\Delta_1\Delta_2\Delta_3 / (x\Delta_1\Delta_3 + y\Delta_1\Delta_2 + \Delta_2\Delta_3) \qquad (4.2.3)$$

where x and y are the ratios of the transition metal thickness and the interfacial reaction layer thickness with respect to the Al-1%Cu thickness. The values of x and y are normally much less than 1.

If, $\Delta_1 < \Delta_2$, $\Delta_1 < \Delta_3$ and $\Delta_2\Delta_3 >> \Delta_1\Delta_3$ and $\Delta_2\Delta_3 >> \Delta_1\Delta_2$,

then, $\Delta = (1+ x + y)\Delta_1$ (4.2.4)

The measured resistivities (Table 4.8) of metallization structures with an extra layer of titanium can be explained by considering that the resistivity of titanium is significantly

higher than that of Al-1%Cu alloy ($\Delta_1 < \Delta_2$) and no interfacial reaction product was detected using XRD. The resistivity of the double-layer metallization structure should be slightly higher than that of the Al-1%Cu alloy according to equation (4.2.4) because almost all the current passes through the Al-1%Cu layer. The situation is different when Ni and Co are used as extra layers. With Ni, a thick reaction product, $NiAl_3$, forms and almost all the current passes through this layer. Owing to formation of reasonably thick layers of $NiAl_3$, the resistivities of Ni/Al-1%Cu bilayer metallization structures have comparatively higher values. This increase in resistance can be minimized however, by reducing the thickness of the nickel layer. In samples where the total Al-Ni thickness was kept at 250 nm, but the nickel layer was reduced to 10 nm thick, the resistance decreased in accordance with the thinner layer of $NiAl_3$ formed. As Table 4.8 shows, the resistivity with 10 nm of Ni was 4.3 and 4.5 microohm-cm for the top and bottom layered schemes respectively. These values are only 10-20% higher than the values measured for the aluminum alloys we used and compare favorably to the resisitivities of the other double layer metallization schemes. An interfacial reaction product, Co_2Al_9, formed in Co/Al-1%Cu films. However due to the slower kinetics of this reaction, the reaction product build-up does not occur as quickly as $NiAl_3$ formation. Resistivities in Co/Al-1%Cu are therefore between those of Ni/Al-1%Cu and Ti/Al-1%Cu.

4.2.4 Conclusions

This work demonstrates the advantages of using bilayer Ni/Al-1%Cu and Co/Al-1%Cu metallization lines in preventing hillock formation. Hillock formation was prevented irrespective of the position (top or bottom) of the nickel layer and PMA treatments, and was effective with a cobalt layer on the bottom when a preheat treatment was applied during deposition. Ti/Al-1%Cu bilayer films also suppress hillock formation, but only when the titanium layer was on the top. Hence metallization procedures with nickel seem more robust compared to strategies using cobalt and titanium bilayer metallization stacks. However, formation of $NiAl_3$ in Ni/Al-1%Cu increases its resistivity. This increase in resistivity can be addressed by reducing the thickness of nickel used in the bilayer; this would control the thickness of the reaction product $NiAl_3$, while retaining the hillock suppression capability of the extra layer of nickel.

4.3 Ohmic Contacts to Indium Tin Oxide

ITO is an essential material in the fabrication of flat panel displays. ITO is so widely used because of its ability to function as a conductor while remaining transparent to visible light [4.3.1]. Active matrix displays, both liquid crystal displays and organic light emitting diode displays, commonly use aluminum (for its low resistivity) as well as ITO in the metallization process [4.3.2]. However, ITO does not form good ohmic contact with aluminum data lines [4.3.3], so barrier layers of third materials such as Cu, Ti, and Pd have been investigated in the past to rectify this problem [4.3.3-5 with varying degrees of success. We have recently reported that the use of an extra layer of nickel or cobalt can successfully eliminate the formation of hillocks in an aluminum metallization scheme [4.3.6]. We propose the use of these materials as barrier layers to form ohmic contacts between aluminum and ITO, in addition to their use as hillock suppression layers. If Ni and Co are to be used as barrier layers in ohmic contact schemes for low temperature

AOLED fabrication, interface reactions in Al-X-ITO (X = Ni, Co) metallization stacks need to be examined.

X-ray photoelectron spectroscopy (XPS), and in some cases X-ray diffraction (XRD) are used in the present work to study these reactions.

4.3.1 Experimental Conditions

The metallization stacks listed in Table 4.10 were prepared and examined by XPS. Samples were prepared on 100 nm oxidized Si wafers of (100) orientation. Aluminum was DC magnetron sputter deposited on Si wafer from a 150 mm diameter aluminum target containing 1% by weight of silicon. This was followed by the deposition of cobalt or nickel barrier layer and then ITO, or just ITO. The multilayer depositions were done without breaking vacuum. RF magnetron sputtered using 150 mm diameter targets, 250 W of power and 9 mTorr of argon as the sputtering ambient. ITO was deposited by RF sputtering from a 150 nm diameter target composed of 90% by weight In_2O_3 and 10% by weight SnO_2 using argon as the sputtering gas. ITO sputter deposition was done at 200 W with a pressure of 3 mTorr. The thickness of each sputtered layer is indicated in Table 4.10. Schematics of the stack structure are presented in Figure 4.14. The metallization stacks were then annealed in vacuum at 400 °C for 30 minutes.

All XPS analysis in this work was conducted using the Scienta Model Esca-300 spectrometer at Lehigh University. Like all dispersion compensated ESCA systems, the Scienta ESCA-300 unit has an x-ray source coupled to a monochromator, an electrostatic lens system, a hemispherical analyzer and a multichannel plate detector which is computer interfaced. For XPS analysis, monochromatic AlK∀ radiation was used. The emitted photoelectrons were collected by a lens system and their kinetic energy was measured with a hemispherical analyzer. The retarding grid of the hemispherical analyzer was scanned in constant analyzer energy mode (CAE) with a pass energy of 150 eV. Under these conditions the energy resolution was 0.4 eV as measured at the Fermi level for Ag. The XPS data consisted of survey scans and regional scans over the photoelectron peaks of interest. For the latter, an energy increment of 0.05 eV was used. Charge correction of the spectra was done by using the adventitious carbon peak, which was set at 285 eV.

Contact scheme	ITO thickness	Barrier layer thickness	Al Thickness
ITO	5 nm	-	-
Al-ITO	5 nm	-	10 nm
Al-Ni-ITO	5 nm	5 nm	10 nm
Al-Ni-ITO	10 nm	5 nm	10 nm
Al-Ni-ITO	8 nm	60 nm	200 nm
Al-Ni-ITO	80 nm	60 nm	200 nm
Al-Co-ITO	5 nm	5 nm	10 nm
Al-Co-ITO	10 nm	5 nm	10 nm

Table 4.10 List of contact schemes examined by XPS

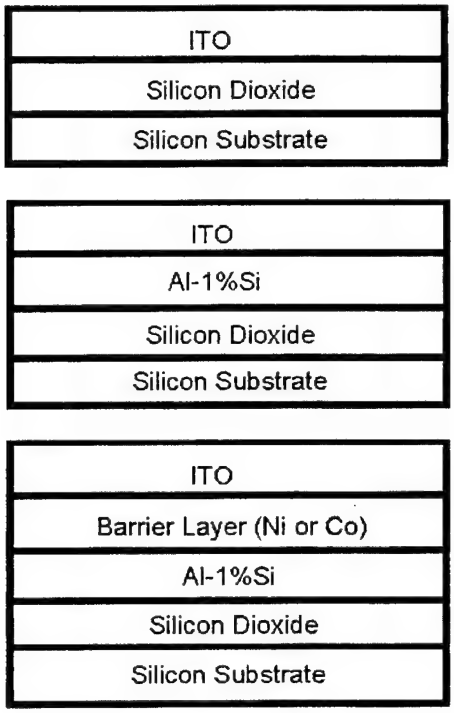


Figure 4.14 Stack structure used in XPS analysis of (a) ITO film, (b) Al-ITO contact, and (c) Al-barrier metal-ITO contact.

4.3.2 Characterization Results

4.3.2.1 ITO

It is important to analyze the spectra obtained from ITO before dealing with reactions in metallization stacks. The Sn-3d, In-3d, and O-1s spectrum obtained from the deposited ITO film are indicated in Figure 4.15, Figure 4.16, and Figure 4.17 respectively. The binding energy positions listed in Table 4.11 are the positions of peak maxima. Two peaks (at 486.7 eV and 495.2 eV) are visible in the Sn-3d (Figure 4.15) spectrum obtained. They are $3d_{5/2}$ and $3d_{3/2}$ x-ray photoelectron lines, respectively. The binding energy of metallic tin and tin oxide are at 484.5 eV and 486.5 eV respectively [4.3.7]. Hence tin (Sn) is in an oxidized environment in the deposited ITO, no metallic tin is present in the deposited film. The In-3d spectrum obtained from deposited ITO (Figure 4.16) also exhibits two peaks like the Sn-3d spectrum due to $3d_{5/2}$ and $3d_{3/2}$ x-ray photoelectron lines. The binding energies of these lines are at 444.7 and 452.2 eV. The peak positions of In-$3d_{3/2}$ and In-$3d_{5/2}$ also suggest that indium is in an oxidized environment. This is in contrast to some of the ITO films, which were deposited by Ishida et al [4.3.8] using electron-beam evaporation where metallic tin and indium were detected. The O-1s spectrum is presented in Figure 4.17. Two distinct peak maxima at

530.4 eV and 532.4 eV are observed in the spectrum obtained from ITO. The O-1s spectrum obtained from the ITO film was also curve fitted using a Voigt function to calculate the curve-fitted peak position and relative fraction of each peak. The curve-fitted peak positions in the O-1s spectrum were at 530.4 eV and 531.6 eV. The binding energy positions of the curve-fitted peak and peak maxima for the lower binding energy peak are identical. They are however considerably different for the higher binding energy peak; besides, this peak is as asymmetric. We therefore concluded that the higher binding energy peak contains a hidden peak. Using a three-peak model during curve fitting (Figure 4.18), the binding energy positions were determined to be 530.4 eV (peak $O\text{-}1s_1$), 531.2 eV (peak $O\text{-}1s_2$) and 532.2 eV (peak $O\text{-}1s_3$). While trying to assign chemical structure to the peaks visible in the O-1s spectrum, it should be noted that the binding energy peak maxima positions in the O-1s spectrum obtained from the ITO film is very similar to what Ishida et al had observed in their film. Ishida et al had proposed their ITO film after deposition consisted of amorphous and microcrystalline ITO, attributing the lower binding energy peak to lattice oxygen in crystalline ITO and the higher binding energy peak to oxygen atoms in an amorphous ITO phase present between the crystalline ITO. The ionicity of oxygen in "amorphous" and "crystalline" environments is different as the ionicity decreases with increasing binding energy. Oxygen in "crystalline" and "amorphous" environments is therefore proposed to contribute to $O\text{-}1s_1$ and $O\text{-}1s_3$ peaks respectively (Table 4.12). Nelson et al's[9] method of deconvolution of the O-1s peak into peaks attributed to O-In and O-Sn bonding was also considered while assigning chemical structure to each deconvoluted peak. The O-Sn peak in Nelson et al's spectrum had a 1.7 eV higher binding energy than the O-In peak. Even though the separation between $O\text{-}1s_1$ and $O\text{-}1s_3$ peaks is 1.8 eV in the ITO film that we deposited (hence, the B.E. difference is very close to that reported by Nelson et al for In-O and Sn-O), it is unlikely that $O\text{-}1s_1$ and $O\text{-}1s_3$ peaks in the O-1s spectrum (Figure 4.18) are due to In-O and Sn-O bonding respectively because the area fraction ratio between $O\text{-}1s_1$ and $O\text{-}1s_3$ is much higher than that expected from ITO. Hence, the possibility of microphase separation in ITO where oxygen atoms are either in a tin rich environment or an indium rich one is ruled out. Based on the observed binding energy positions of peaks in the spectrum, we can also rule out the possibility that any of the three peaks is due to hydroxide formation [4.3.10-11]. Since, elemental tin and indium are not detected in out ITO film, the possibility of any peak forming due to adsorbed oxygen on a metal surface [4.3.10] does not arise. Presence of suboxides of ITO in crystalline or amorphous environment can cause tailing of O-1s peaks attributed to stoichiometric ITO on the higher binding energy side. The possibility that suboxide formation has contributed to the presence of peak $O\text{-}1s_2$ cannot therefore be ruled out. However even if suboxides did form, they did not do so in significant quantities. Otherwise, their presence would also be indicated in the In-3d and Sn-3d spectra. Summing up, peaks in the O-1s spectra are proposed to arise from the different types of structural oxygen present in ITO proposed by Ishida et al[8] which was mentioned earlier, with each structural type having a different ionicity; ITO suboxide formation may have also influenced the shape of the O-1s spectrum somewhat, with the most significant influence possibly being on peak $O\text{-}1s_2$.

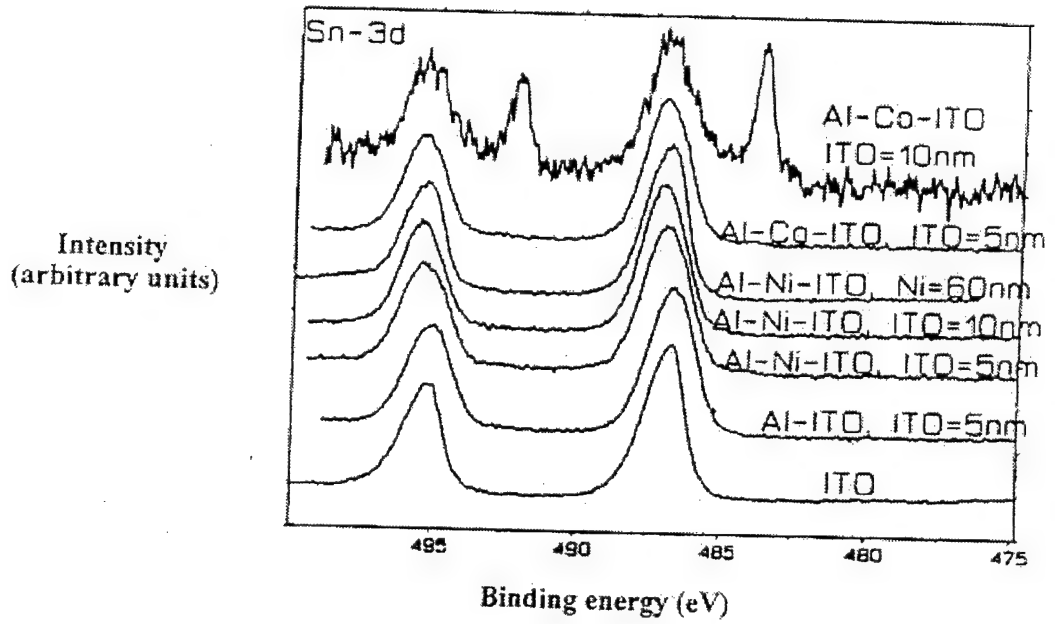


Figure 4.15 Sn-3d x-ray photoelectron spectra

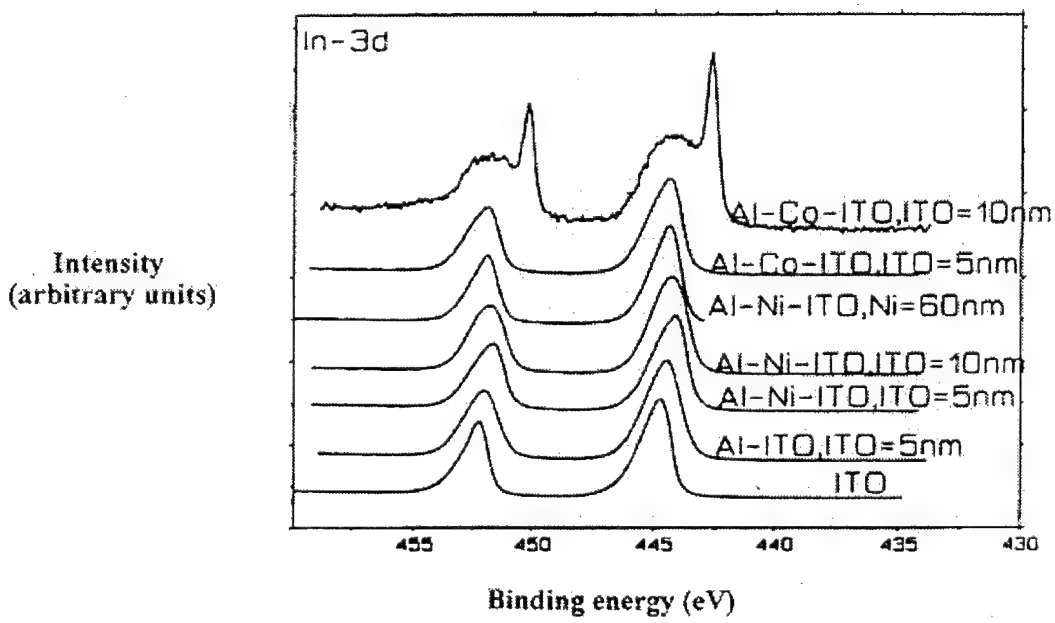


Figure 4.16 In-3d x-ray photoelectron spectra

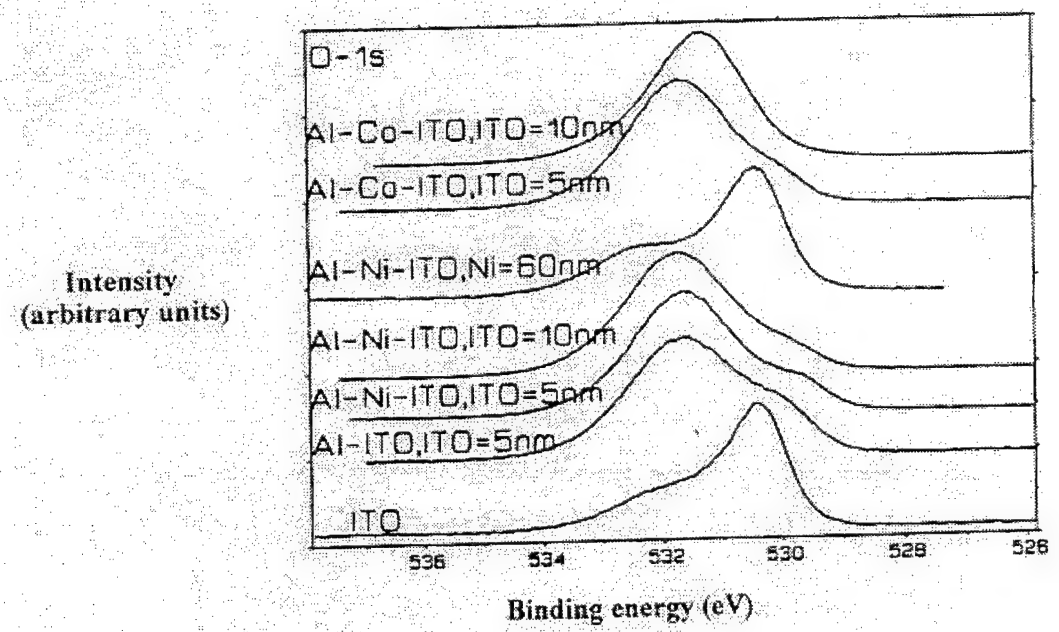


Figure 4.17 O-1s x-ray photoelectron spectra

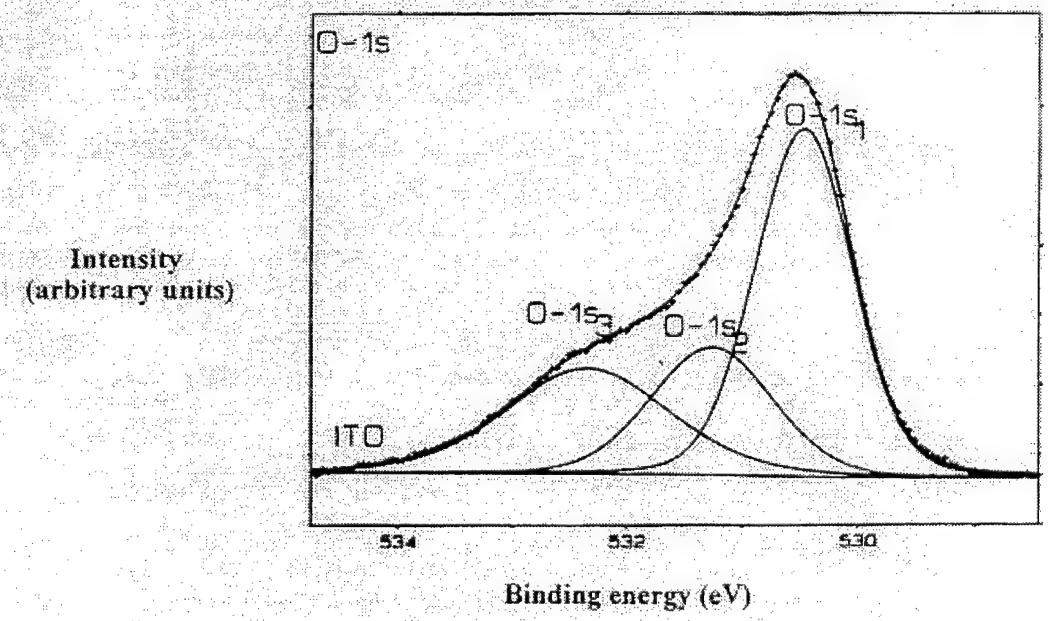


Figure 4.18 Voigt function fit of O-1s spectra obtained from ITO

XPS spectrum	Peak Number	ITO	Al-ITO	Al-Ni-ITO	Al-Ni-ITO	Al-Ni-ITO	Al-Co-ITO	Al-Co-ITO
			ITO = 5nm Al = 10nm	ITO = 5nm Ni = 5nm Al=10nm	ITO = 10nm Ni = 5nm Al = 10nm	ITO = 8nm Ni = 60nm Al = 200nm	ITO = 5nm Co = 5nm Al = 10nm	ITO = 10nm Co = 5nm Al = 10nm
In-3d	1	444.7	444.4	444.1	444.2	444.4	444.3	442.7
	2	452.2	452.5	451.9	451.9	452.1	451.8	444.3
	3							450.3
	4							452.0
Sn-3d	1	486.7	486.8	486.9	487.1	486.5	487.1	483.7
	2	495.2	495.1	495.5	495.5	494.9	495.5	487.0
	3							492.1
	4							495.4
O-1s	1	530.4	529.9	529.6	529.7	530.4	529.9	531.3
	2	532.4	531.7	531.6	531.7	532.4	531.7	
Al-2p	1		71.9	72.2	72.2	-	72.2	71.8
	2		74.9	74.9	75.0	-	74.8	74.6
Ni-2p	1			852.8	852.8	852.8		
	2			870.0	870.0	870.0		
Co-2p	1						780.9	777.4
	2							780.9
	3							

Table 4.11 Binding energies of XPS peak (peak maxima positions) in eV

4.3.2.2 Al-ITO Reaction

Let us now examine the spectra obtained from the Al-ITO metallization stack where Al-1%Si and ITO layer thicknesses are 5 nm and 10 nm respectively. There is no significant change in the binding energies of peaks obtained from Sn-3d (Figure 4.15) and In-3d (Figure 4.16) spectra compared to those obtained from the ITO film. However a distinct change is visible in the O-1s spectrum (Figure 4.17) obtained from the Al-ITO metallization stack. The relative fraction of the O-$1s_1$ peak (Table 4.11) has dropped considerably compared to the same peak in the O-1s spectrum obtained from the ITO film. Since the O-$1s_1$ peak is due to "lattice" oxygen in ITO, it is clear that metal-oxygen bonds in microcrystalline ITO have been broken and the released oxygen has partly reacted with Al to form Al_2O_3 and also found itself a less ionic environment. This is evident from the increase in relative intensity of the O-$1s_3$ peak. Increase in relative intensity of the O-$1s_3$ and O-$1s_2$ peaks may also be caused by ITO suboxide formation through reaction as discussed later. Formation of Al_2O_3 at the Al-ITO interface is confirmed after examining the Al-2p spectrum (Figure 4.19) The spectrum indicates two peaks at approximately 72 eV and 75 eV for separate chemical species. The spin-orbit photoelectron lines are distinctly resolved in the lower binding energy peak. The lower binding energy peak (the peak, which shows a distinct spin-orbital split at approximately 72 eV,) is due to Al^0 and the higher binding energy peak (at approximately 75 eV) is due to Al^{3+} [12]. Calculation of)G at 400° C for Al_2O_3, SnO_2 and In_2O_3 using thermodynamic data provided by Barin et al[13] indicates that Al_2O_3 is more stable than SnO_2 or In_2O_3.

$$4/3\ Al + O_2 = 2/3\ Al_2O_3\ ()G = -971)$$

$$4/3\ In + O_2 = 2/3\ In_2O_3\ ()G = -467)$$

$$Sn + O_2 = SnO_2\ ()G = -579)$$

Hence Al_2O_3, which forms at the Al/ITO interface in Al-ITO stacks, occurs by direct displacement type redox reaction. However, direct redox reaction does not cause metallic tin or indium to form at the interface. The reaction is of the following nature

$$2Al + xSnO_2.yIn_2O_3 = Al_2O_3 + xSnO_{2-a}.yIn_2O_{3-b}, \text{ where } ax + by = 3$$

Considerable rearrangement of metal-oxygen bonds in ITO occur as a result of this reaction. The above reaction is important because formation of Al_2O_3 at the Al-ITO interface prevents ohmic contact between Al and ITO in Al-ITO metallization stacks [4.3.14].

Contact scheme specimen	Peak O-$1s_1$		Peak O-$1s_2$		Peak O-$1s_3$	
	B.E. (eV)	% Peak fraction	B.E. (eV)	% Peak fraction	B.E (eV)	% Peak fraction
ITO	530.4	50	531.2	23.2	532.2	26.3
Al(10nm)-ITO (5nm)	529.9	15.1	531.1	24.8	531.9	60.2
Al (10nm)-Ni(5nm)-ITO (5nm)	529.8	10	531.1	17.3	531.8	76.0
Al(10nm)-Ni(5nm)-ITO (10nm)	529.8	6.6	531.0	11.7	531.8	81.7
Al(200nm)-Ni(60nm)-ITO(8nm)	530.1	55.2	531.2	15.8	532.2	28.1
Al(10nm)-Co(5nm)-ITO (5nm)	529.9	6.9	531.0	17.4	531.8	76.0
Al(10nm)-Co(5nm)-ITO (10nm)	530.5	6.6	531.3	56.1	532.1	19.7

Table 4.12 Binding energies of deconvoluted peaks and peak area fractions in O-1s spectrum obtained from ITO film

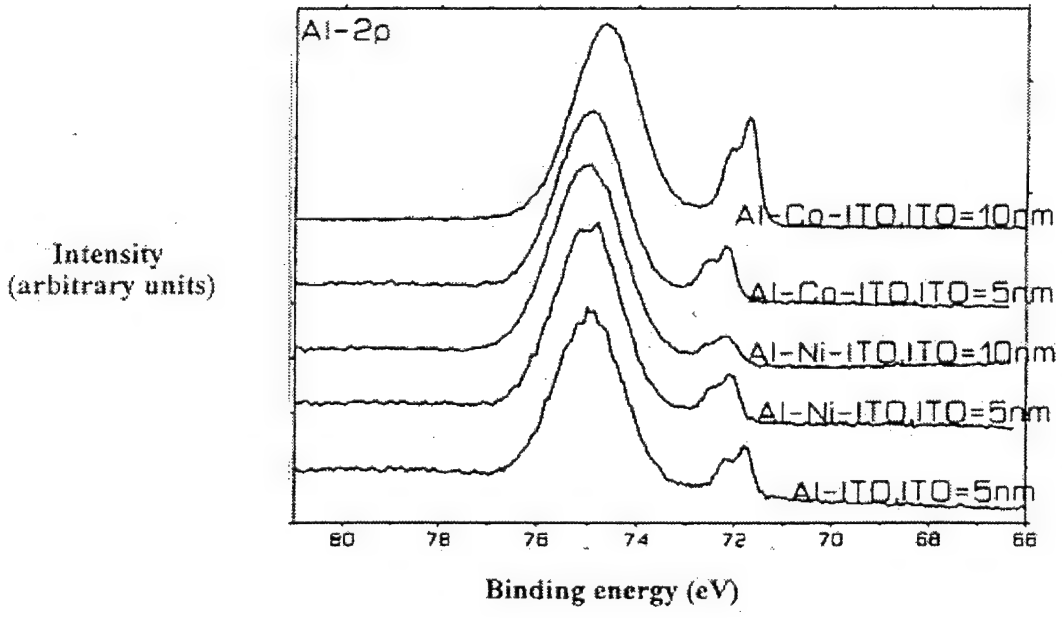


Figure. 4.19 Al-2p x-ray photoelectron spectra

4.3.2.3 Al-Ni-ITO Reaction

Sn-3d (Figure 4.15) and In-3d (Figure 4.16) spectra obtained from any of the Al-Ni-ITO metallization stacks which were examined in this study are not significantly different from the respective spectrum obtained the Al-ITO metallization stack, which was discussed in the previous section. Even the O-1s and Al-2p spectra obtained from specimens with a thin barrier layer (<10 nm) of Ni are similar. These results indicate that if the Ni barrier layer is thin, Al_2O_3 forms through reaction in Al-Ni-ITO metallization stacks owing to diffusion of oxygen through the barrier layer. The Ni-2p spectrum obtained from Al-Ni-ITO metallization stack with a thin barrier layer (Figure 4.20) indicated that Ni did not participate in reactions at the Ni-ITO interface. To obtain ohmic contact at Al-Ni-ITO metallization stacks, the thickness of the Ni barrier layer had to be increased, so that oxygen could not diffuse through the barrier layer. The O-1s spectrum obtained from Al-Ni-ITO metallization stack with a thick barrier layer (60 nm of Ni) is indicated in Figure 4.17. Since no reaction has occurred at the Ni-ITO interface, the relative fraction of the $O\text{-}1s_I$ peak is similar to that obtained from ITO. The Al layer in the Al-Ni-ITO stack with a thick Ni barrier layer was below the escape depth of Al-2p photoelectrons, hence we examined the Al-Ni interface in this specimen using x-ray diffraction (XRD) instead of XPS. The XRD pattern (Figure 4.21) also indicates that a thicker Ni barrier layer causes Al_3Ni to form at the Al-Ni interface in Al-Ni-ITO stacks. However, Al_3Ni formation does not have any deleterious effects with regard to formation of ohmic contacts [4.3.14]. Figure 4.22 depicts resistance measurements made along a transfer length structure for an Al-Ni-ITO contact scheme using 50 nm of nickel sandwiched between 100 nm of ITO and 200 nm of Al. The sample underwent two anneals at 400° C for 30 minutes in 90% N_2- 10% H_2. Ohmic contacts were successfully formed, with a measured specific contact resistance of 40-100 Ohm-cm^2 after these anneals.

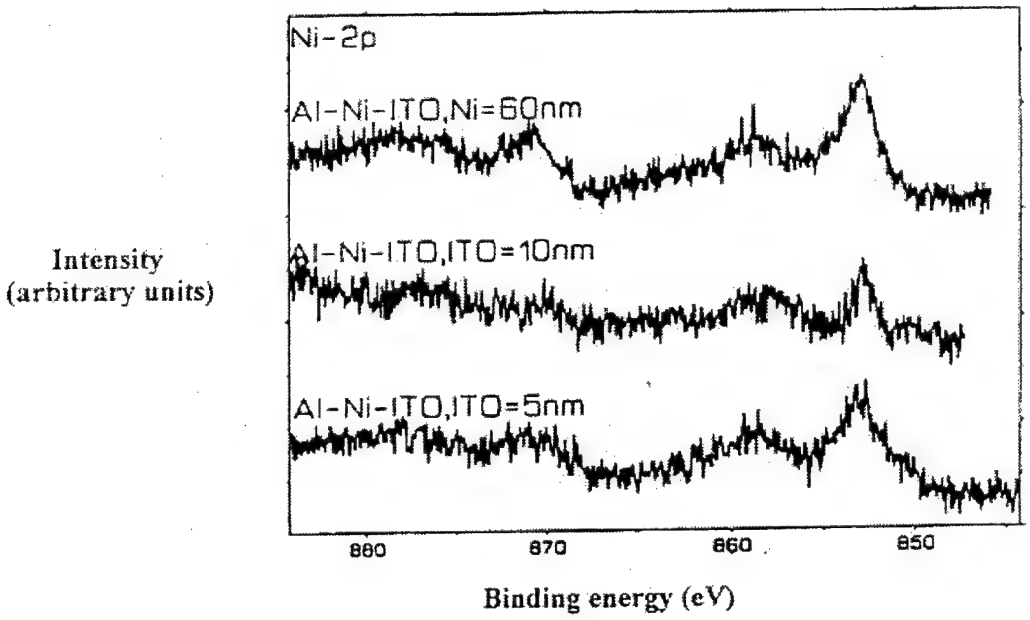


Figure 4.20 Ni-2p x-ray photoelectron spectra from Al-Co-ITO sample

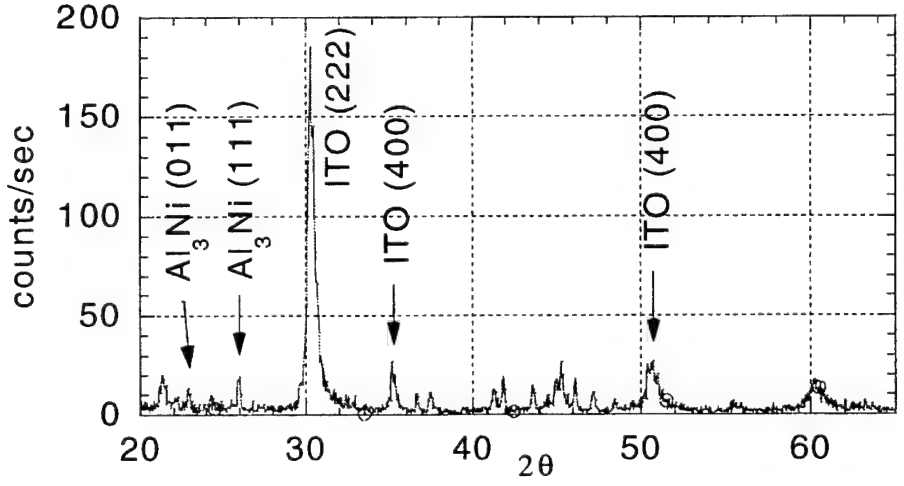


Figure 4.21 XRD patterns of Al-Ni-ITO stack with 200 nm of Al, 60 nm of Ni and 800 nm of ITO. Al_3Ni is the only intermetallic detected.

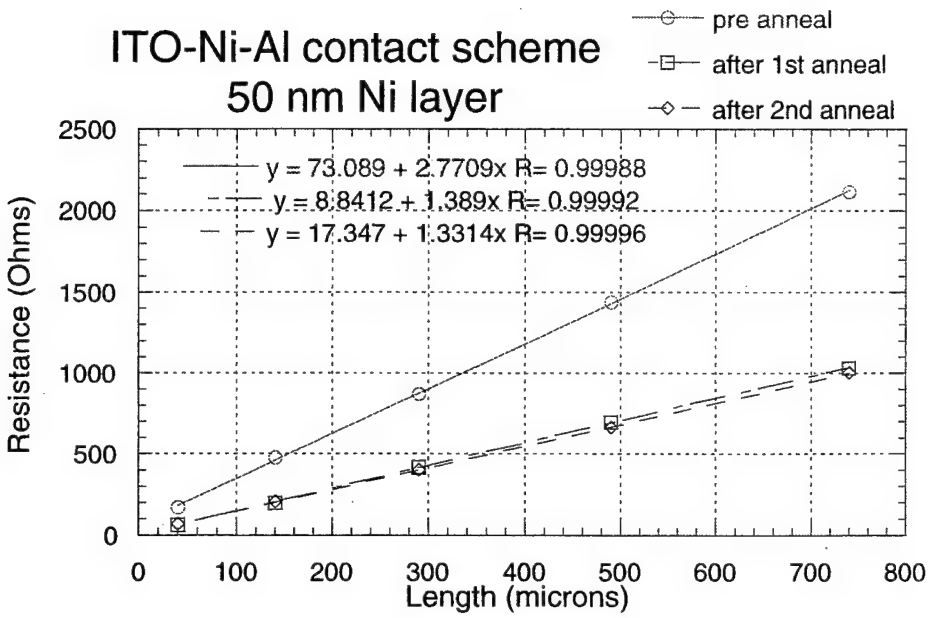


Figure 4.22 Transfer length structure measurement for ITO-Ni-Al (50 nm of Ni). Contact size is 50 μm by 10 μm

4.3.2.4 Al-Co-ITO Reaction

The Sn-3d (Figure 4.15) and In-3d (Figure 4.16) obtained from the Al-Co-ITO metallization stack with a 5 nm Co barrier layer and 5 nm thick ITO layer is similar to those obtained from Al-ITO and Al-Ni-ITO stacks. However, when the ITO layer thickness was increased to 10 nm, a significant change occurred in both Sn-3d and In-3d spectra. In the Sn-3d spectrum (Figure 4.15), extra peaks were visible at 483.7 eV and 492.1 eV while in the In-3d spectrum new peaks were observed at 444.7 eV and 452.2 eV. The new peaks in both spectra occur due to formation of reduced Sn and In species due to reaction at the Co-ITO interface. Cobalt oxides are more stable than SnO_2 or In_2O_3, hence cobalt cannot directly reduce indium or tin oxides in ITO through displacement type redox reactions. Interface reactions can only be initiated through alloying that occur because of interdiffusion between indium, tin and barrier layer Co atoms. Break-up of metal-oxygen bonds in crystalline ITO occurs yielding Co-Sn, Co-In, or Co-Sn-In intermetallics at the Co-ITO interface. The released oxygen diffuses through the barrier layer and subsequently reacts with aluminum to form Al_2O_3. In spite of Al_2O_3 formation in Al-Co-ITO stacks with thin barrier layers of Co, it was found that it was still possible to obtain ohmic contacts in these metallization stacks (unlike in Al-Ni-ITO stacks with very thin Ni barrier layers) [4.3.14].

Figure 4.23 depicts resistance measurements made along a transfer length structure for an Al-Co-ITO contact scheme using 10 nm of cobalt sandwiched between 100 nm of ITO and 200 nm of Al. The sample underwent two anneals at 400° C for 30 minutes in 90% N_2- 10% H_2. Ohmic contacts were formed, with a measured contact resistance of 60-100 ohms after the anneals. The ohmic contacts were formed in this scheme due to the reduced intermetallic species (Co-Sn or Co-In or Co-In-Sn compound), which formed at the Co-ITO interface through reaction. From the Co-2p spectrum (Figure 4.24), it is

clear that interfacial reaction products such as cobalt oxides did not form at the interface after Al-Co-ITO stacks were annealed. Intermetallics also did not form at the Co-Al interface unlike that observed at the Ni-Al interface in Al-Ni-ITO stacks. This can be attributed to the comparatively slower kinetics of intermetallic alloy formation in the Co-Al system [4.3.6].

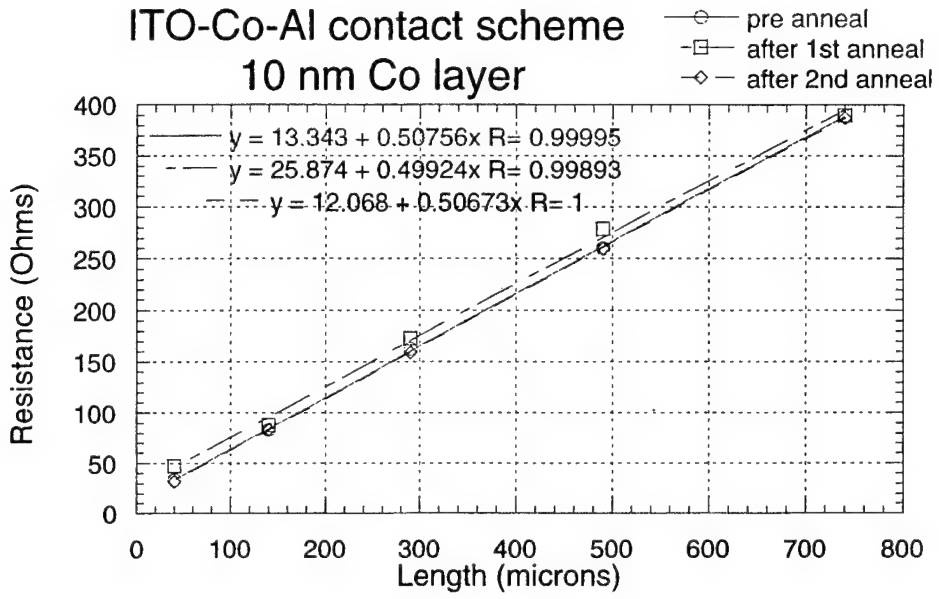


Figure 4.23 Transfer length structure measurement for ITO-Co-Al (10 nm of Co). Contact size is 50 μm by 10 μm

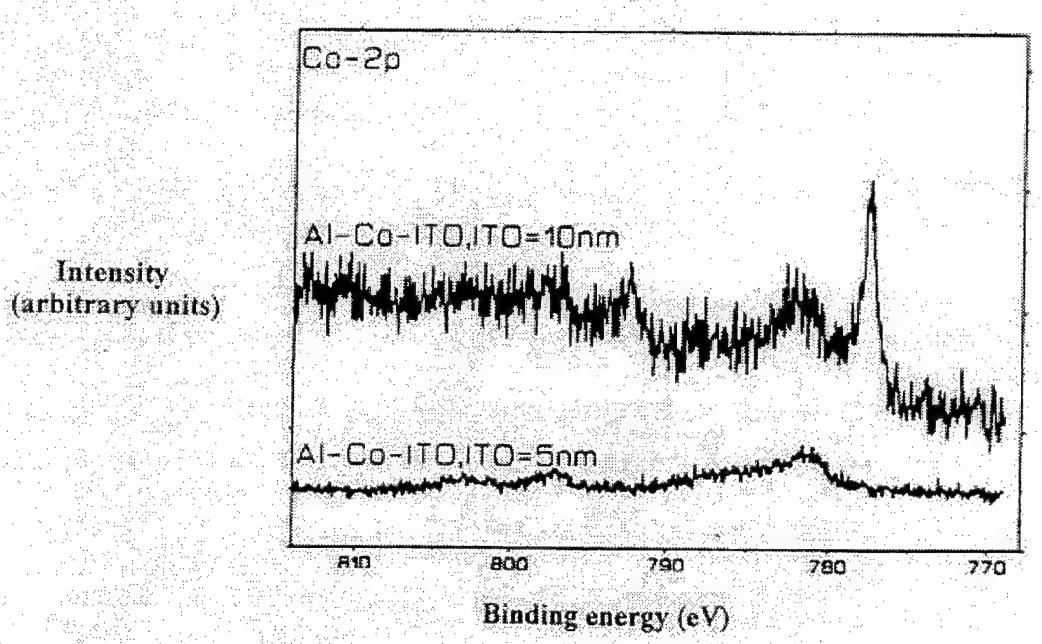


Figure 4.24 Co-2p x-ray photoelectron spectra from Al-Co-ITO sample.

4.3.3 Conclusions

XPS analysis was performed on sputter deposited ITO and Al-ITO metallization stacks with and without barrier layers (Ni and Co). In Al-ITO interfaces, Al_2O_3 formed through reaction, which led to non-ohmic contact development. In Al-Ni-ITO metallization stacks, reaction occurred at the Al-Ni interface (leading to formation of Al_3Ni) and not at the Ni-ITO interface. Ohmic contacts could only be obtained when the barrier Ni layer was sufficiently thick to prevent diffusion of oxygen through the barrier layer so that Al_2O_3 formation was prevented. However, in Al-Co-ITO stacks, the primary reaction that led to ohmic contact formation occurred at the Co-ITO interface where reduced intermetallic Sn and In species formed as a result of reaction. Hence even with thin Co barrier layers, ohmic contact was obtained in Al-Co-ITO metallization stacks.

5. Future Work

The field of large area electronics is rapidly growing. There are many applications that would not be feasible if the polysilicon material could not be crystallized at glass compatible temperature. Likewise, there are currently many applications that are not being realized because a low cost polysilicon crystallization process has not been developed for temperatures compatible with flexible plastic substrates. One goal of future work may be to develop new processes that further reduce the process temperature of large area electronics without increasing the process cost.

Further work can also be done to improve the performance of polysilicon devices using existing processes. This work has shown that the device performance is a function, not only of the polysilicon grain size, but also of the level of intra-grain defects. More work needs to be done to improve the grain structure for a given grain size in order to improve the performance of the polysilicon TFTs.

This work has demonstrated circuit components using a low cost, high throughput polysilicon process. More work needs to be done to investigate the reliability of these circuits as well as the realization of more complex circuit blocks such as a display data driver. Furthermore, novel circuit designs can be integrated at the pixel level to ease the drive requirements of the display or to provide pixel amplification for lower noise detectors.

6. Glossary

AFM	atomic force microscopy
AMLCD	Active Matrix Liquid Crystal Display
AMOLED	Active Matrix Organic Light Emitting Diode
DAC	digital to analog converter
DFF	D Flip Flops
DI	deionized water
ELA	excimer laser annealing
GA-XRD	glancing angle x-ray diffraction
IPA	isopropanol alcohol
ITO	indium tin oxide
LCD	liquid crystal display
LDD	lightly doped drain
LPCVD	low pressure chemical vapor deposition
OLED	organic light emitting diode
PECVD	plasma enhanced vapor deposition
RTP	Rapid Thermal Processing
SEM	scanning electron microscope
SOG	spin on glass
TEM	tunneling electron microscope
TFT	thin film transistor
VLSI	very large scale integrated
XPS	x-ray photoelectron spectroscopy
XRD	x-ray diffraction

7. References

[1.1] Y. Morimoto et. al., "A 2.4" Driver-Integrated Full-Color QVGA Polysilicon-Si TFT LCD by a Novel Low Temperature Process Using a Combination of ELA and RTA Technology." IEDM '95 Digest, 837, (1995).

[1.2] A. T. Voutsas, "Enhanced grain growth phenomena in excimer laser annealed microcrystalline silicon films." Jpn. Jn. Appl. Phys. **37**, 388 (1998).

[1.3] H. Hovagimian, J. Mehlhaff, S. Oresman, "Recent Advances in RTP Processing of Polysilicon LCDs." SID International Display Research Conf., M52, (1997).

[1.4] M. Hatalis, D. Greve. "Large Grain Polycrystalline Silicon by Low Temperature Annealing of Low Pressure Chemically Vapor Deposited Amorphous Silicon Films." Journal of Applied Physics. **63**, 2260 (1988).

[1.5] Wolf and Tauber. Silicon Processing for the VLSI Era. Lattice Press. 618 (1986).

[1.6] R. L. Plackett and J. P. Burman, Biometrika, **33**, 305 (1946).

[1.7] A. I. Khuri and J. A, Cornell, Response Surface Design and Analysis. Marcell Dekker, NY (1987).

[1.8] G. Sarcona, M. Stewart, M. K. Hatalis, " Polysilicon Thin Film Transistors using Self-Aligned Cobalt and Nickel Silicide Source and Drain Contacts." Electron Device Letters, **20**, 332 (1999).

[1.9] D.N. Kouvatsos, A.T. Voutsas, M.K. Hatalis, "High Performance Thin Film Transistors in Large Grain Size Polysilicon Deposited by the Thermal Decomposition of Silane." IEEE Transaction on Electron Devices, **43**, 1399, (1996).

[1.10] J. Leveinson, F.R. Shepherd. P.J. Scanlon, W.D. Westwood, G. Este, and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors." J. Applied Physics, **53**, 1193 (1982).

[1.11] G. Baccarani, B. Ricco. "Transport Properties of Polycrystalline Silicon Films." J. Appl. Phys., **49**, 5565 (1978).

[1.12] J. Fossom, A Ortiz-Conde, H. Shichijo, S.K. Banarjee. "Anomalous Leakage Current in LPCVD Polysilicon MOSFETs." IEEE Trans. On Elec. Dev., **32**, 1878 (1985).

[1.13] G-Y. Yang, S-H. Hur, C-H. Han. "A Physically-Based Analytical Turn-On Model of Polysilicon Thin-Film Transistors for Circuit Simulation." IEEE Trans. On Elect. Dev., **46**, 165 (1999).

[2.1] I.D. Parker. "Carrier Tunneling and device characteristics in polymer light emitting diodes." J. Appl. Phys., **75**, 1656 (1994).

[2.2] C.W. Tang. "An Overview of Organic Electroluminescent Materials and Devices." SID '96 Digest, 181 (1996).

[2.3] J.C. Sturm, C.C. Wu. "Integrated Organic Light Emitting Diode Structures Using Doped Polymers." IDRC '97 Digest, F-11 (1997).

[2.4] M.K. Hatalis, M. Stewart, C.W. Tang, and J. Burtis. "Polysilicon TFT Active Matrix Organic EL Displays." SPIE, **3057**, 277 (1997).

[2.5] R.M.A.Dawson et al. "Design of an Improved Pixel for a Polysilicon Active Matrix Organic EL Display" SID '98 Digest, 4.2 (1998).

[2.6] C. W. Tang, S.A. VanSlyke. "Organic Electroluminescent Diodes." Appl. Phys. Lett. **51**, 913 (1987).

[2.7] H. Hovagimian, J. Mehlhaff, S. Oresman. "Recent Advances in Rapid Thermal Processing of Polysilicon TFT LCDs." IDRC Conference Digest, M-52 (1997).

[2.8] G. Sarcona, M. Stewart, M. K. Hatalis. "Polysilicon Thin Film Transistors with Cobalt and Nickel Silicide Source and Drain Contacts." Electron Device Letters, **20**, 332 (1999).

[2.9] R Howell, G.T. Sarcona, and M.K.Hatalis. "Preparation and Stability of Low Temperature Cobalt and Nickel Silicides on Thin Polysilicon Films." Submitted to Journal of Vacuum Science (1999).

[2.10] S. Saha, R. Howell, M. K. Hatalis. "Elimination of Hillock Formation in Al Interconnects Using Co, Ni Interlayers." Journal of Applied Physics, **86**, 625 (1999).

[2.11] R. Howell, S. Saha, and Miltiadis K. Hatalis. "Cobalt and Nickel for Improved Aluminum-Indium Tin Oxide Contact Metallurgy in Polysilicon TFT Display Applications." Mat. Res. Soc. Sym. Proc., **508**, 321 (1998).

[2.12] M. Stewart, R. Howell, L. Pires, M.K. Hatalis, O.Prache, and W. Howard. "Polysilicon VGA Active Matrix OLED Displays - Technology and Performance." IEDM '98 Proceedings, 871 (1998).

[3.1] Alan Lewis, D.Lee, R. Bruce. "Polysilicon TFT Circuit Design and Performance." IEEE Journal of Solid State Circuits, **27**, 1833 (1992).

[3.2] M. Stewart, L.Pires, R. Howell, M. Hatalis, O. Prache, W. Howard, "Polysilicon VGA Active Matrix OLED Displays – Technology and Performance." IEDM Proceedings 1998, 871 (1998).

[3.3] R.M.A. Dawson et al. "Design of an Improved Pixel for a Polysilicon Active Matrix Organic EL Display." SID '98 Digest, 4.2 (1998).

[3.4] H. Hovagimian and J. Melhlaff. "Recent advances in Rapid Thermal Processing of Polysilicon TFT LCDs." IDRC Conference Digest, M-52 (1997).

[3.5] M. Stewart, H. Hovagimian, J. Arakkal, S. Saha, Miltiadis K. Hatalis. "Low Temperature PECVD Polysilicon Crystallization by Rapid Thermal Processing." Mat. Res. Soc. Symp. Proc., **508**, 109 (1998).

[3.6] S.M. Fluxman. "Design and Performance of Digital Polysilicon thin-film-transistor Circuits on Glass." IEE Proc.-Circuits Devices and Systems, **141**, 56 (1994).

[3.7] R. Gregorian, W.E. Nicholsan. "CMOS Switched- Capacitor Filters for a PCM Voice CODEC." IEEE Journal of Solid State Circuits, **14**, 970 (1979).

[3.8] Y. Aoki et al. "A 10.4" XGA Low Temperature Polysilicon TFT-LCD for Mobile PC Applications." SID Digest '99, 176 (1999).

[3.9] M.K. Hatalis, M. Stewart, C.W. Tang, and J. Burtis. "Polysilicon TFT Active Matrix Organic EL Displays." SPIE, **3057** , 277 (1997).

[3.10] R.M.A.Dawson et al. "Design of an Improved Pixel for a Polysilicon Active Matrix Organic EL Display" SID Digest '98, 4.2 (1998).

[3.11] M. Stewart, H. Hovagimian, J. Arakkal, S. Saha, Miltiadis K. Hatalis. "Low Temperature PECVD Polysilicon Crystallization by Rapid Thermal Processing." Mat. Res. Soc. Symp. Proc., **508**, 109 (1998).

[3.12] A. Lewis, D.Lee, R. Bruce. "Polysilicon TFT Circuit Design and Performance." IEEE Journal of Solid State Circuits. **27**, 1833 (1992).

[3.13] S.M. Fluxman. "Design and Performance of Digital Polysilicon thin-film-transistor Circuits on Glass." IEE Proc.-Circuits Devices and Systems, **141**, 56 (1994).

[3.14] S. Seki, O. Kogure, B. Tsujiyama, "Laser Recrystallized Polycrystalline-Silicon Thin Film Transistors with low leakage Current and High Switching Ratios." IEEE Electron Device Letters, **8**, 425 (1987).

[3.15] T. Zhao, M. Cao, J. Plummer, K. Saraswat. "A Novel Floating Gate Spacer Polysilicon TFT." IEDM '93 Digest, 392 (1993).

[3.16] Byung-Hyuk Min, C-M. Park, M-K. Han. "A PN Gate Polysilicon Thin Film Transistor." IEDM '95 Digest, 834 (1995).

[4.1.1] G.T. Sarcona, M.K. Hatalis. "Low Temperature Silicides for Poly-Silicon Thin Film Transistor Applications." Materials Res. Soc. Symposium Proc. 402, (1996).

[4.1.2]. W. H. Dumbaugh, P. L. Bocko, Society for Information Display Digest of Technical Papers 1990, 21, 70, (1990).

[4.1.3]. H. Jiang, C.M. Osburn, P. Smith, Z.-G. Xiao, D. Griffis, G.M. M^{C} Guire, G.A. Rozgonyi. "Ultra Shallow Junction Formation Using Diffusion from Silicides: I. Silicide Formation, Dopant Implantation and Depth Profiling." J. Electrochem. Soc. 139, 196 (1992).

[4.1.4]. H. Jiang, C.M. Osburn, Z.-G. Xiao, G.M. M^{C} Guire, G.A. Rozgonyi. "Ultra Shallow Junction Formation Using Diffusion from Silicides: II: Diffusion in Silicides and Evaporation." J. Electrochem. Soc. 139, 206 (1992).

[4.1.5] W.J. Freitas, J.W. Swart. "Influence of Impurities on Cobalt Silicide Formation." J. Electrochem. Soc. 138, 3067 (1991).

[4.1.6] H. Mishima, T. Yasui, T. Mizuniwa, M. Abe, T. Ohmi, "Particle-Free Wafer Cleaning and Drying Technology." IEEE. Trans. Semiconductor Manufacturing. 2, 69, (1989).

[4.1.7] H. Mishima, T. Ohmi, T. Mizuniwa, M. Abe, "Deposition Characteristics of Isopropanol (IPA) and Moisture from IPA Vapor Dried Silicon Wafers." IEEE. Trans. Semiconductor Manufacturing. 2, 121, (1989).

[4.1.8] F. La Via, A. Alberti, V. Raineri, S. Ravesi, E. Rimini, "Thermal Stability of thin $CoSi_2$ layers on polysilicon implanted with As, BF2 and Si." Vac. Sci. Technol. B. 16, 1129, (1998).

[4.1.9] K. Maex. MRS Fall 1995 Silicide Technology Lecture Notes.

[4.1.10] T. Morimoto, T. Ohguro, H.S. Momose, T. Iinuma, I. Kunishima, K. Suguro, I. Katakabe, H. Nakajima, M. Tsuchiaki, M. Ono, Y. Katsumata, H. Iwai, "Self-Aligned Nickel-Mono-Silicide Technology for High-Speed Deep Submicrometer Logic CMOS ULSI," IEEE Trans. Electron Dev. 42, 915, (1995).

[4.1.11] R. Pretorius, "Prediction of Silicide Formation and Stability using Heats of Formation," Thin Solid Films, 290-291, 482, (1996).

[4.1.12] M. Stewart, Ph.D. Dissertation, Lehigh University (1999).

[4.2.1] A.F. Puttlitz, J.G. Ryan, T.D. Sullivan, IEEE Transactions on Components, Hybrids and Manufacturing Technology. 7 (12), 619 (1989).

[4.2.2] E.P. van de Ven, R.S. Martin and M.J. Berman in Proceedings of the Fourth International IEEE VLSI Multilevel Interconnection Conference, Santa Clara, CA, USA, 15-16 June, 1987.

[4.2.3] A.A. Brown, K.B. Affolter, S.R. Jennings and P.J. Rosser in Proceedings of the Fourth International IEEE VLSI Multilevel Interconnection Conference, Santa Clara, CA, USA, 15-16 June, 1987.

[4.2.4] T. Ericsson, J. Vac. Sci. Technology. B 9 (1), 58 (1991).

[4.2.5] S. Aceto, C.Y. Chang and R.W. Vook, Thin Solid Films, 219, 80 (1992).

[4.2.6] M. Hayashi, K. Inoue, S. Noumi, K. Sakata, T. Takeguchi, T. Morita and T. Eguchi, Society for Information Display'97 Digest (SID, Santa Ana, California, 1997), p 885.

[4.2.7] T. Onishi, E. Iwamura, K. Takagi and K. Yoshikawa, J. Vac. Sci. Technology. A 14 (5), 2728 (1996).

[4.2.8] E. Iwamura, T. Ohnishi and K. Yoshikawa, Thin Solid Films 270, 450 (1995)

[4.2.9] T. Onishi, E. Iwamura, K. Takagi and T. Watanabe, J. Vac. Sci. Technology A 15 (4), 2339 (1997).

[4.2.10] Y.K. Lee, N. Fujimura, T. Ito and N. Nishida, J. Vac. Sci and Technology B 9 (5), 2542 (1991).

[4.2.11] Y. Zhao, S. Xiong, C. Gu, Z.P. Wang, Z. Zhou, Z. Meng, J. Li, Y. Dai, L. Yao, J.J. Zhang, S. Ding, Z.L. Sun, W.D. Geng, H.Y. Li and D.L. Li, Society for Information Display'96 Digest (SID, Santa Ana, California, 1996), p345.

[4.2.12] T. Kawamura, K. Fujii, K. Honda, K. Iwasaki, T. Tamura, H. Koseki, S. Hotta, J. Institute. Television. Engineers. Jpn, 147 (5), 630 (1993).

[4.2.13] H. Onoda, E. Takahashi, Y. Kawai, S. Madokaro, H. Fukuyo and S. Sawada, Jpn.J.App.Phys 32 (11a), 4934 (1993).

[4.2.14] D.S. Gardner, T.L. Michalka, K.C. Saraswat, T.W. Barbee, and J.D. Meindl, International Symposium on VLSI Technology, Systems and Applications (Nat. Sci. Council. Ind. Tech. Res. Inst ERSO Hsinchu, Taiwan, 1985) p 157.
[4.2.15] D.S. Gardner, T.L. Michalka, K.C. Saraswat, T.W. Barbee, J.P. McVittie and J.D. Meindl, IEEE Journal of Solid-State circuits, SC-20 (1), 94 (1985).
[4.2.16] R.S. Howell, S.K. Saha and M.K. Hatalis, presented at the Flat Panel Display Materials Symposium (Materials Research Society, San Fransisco, CA, April 1998).
[4.2.17] S. Wolf and R.N. Tauber in Silicon Processing for the VLSI era, Volume 1-Process Technology (Lattice Press, Sunset Beach, California, 1986), p 361
[4.2.18] R.J. Wilson and B.L. Weiss, Vacuum, 42 (12), 719 (1991)
[4.2.19] P. Chaudhury, J.Appl. Phys, 45 (10), 4339 (1974)
[4.2.20] F.R.N. Nabarro, Proceedings of the Conference on the Strength of Solids (The Physics Society, London, 1948) pp 75.
[4.2.21] M.F. Ashby, Acta Metallurgica, 20, 887 (1972)
[4.2.22] J. Krol, Materials Science and Eng A, 169 (1997)
[4.2.23] D.S. Gardner and P.A. Flinn, J. Appl. Phys, 67 (4), 1831 (1990)
[4.2.24] K.Y. Gao and B.X. Liu, Nucl. Inst. Methods. Phys. Res B 132, 68 (1997)
[4.3.1] A.J.P. Theuwissen and G.J. Declerk, Thin Solid Films, 121 (2), 109 (1984)
[4.3.2] L.E. Tannas, Flat Panel Display and CRTs, (Van Nostrand Reinhold, New York, USA, 1985)
[4.3.3] D.M. Brown, M. Ghezzo and P.L. Sargent, IEEE. Trans. Elect. Dev, 25, 79 (1978)
[4.3.4] R.W. Birkmire, B.E. McCandless and W.N. Shafermann, Solar Cells, 23, 115 (1988)
[4.3.5] C.H.L. Witjens and P.A.C. Van Loon, J.Electrochem. Soc, 137 (12), 3928 (1990)
[4.3.6] S.K. Saha, R.S. Howell and M.K. Hatalis, J. Appl Phys (in print)
[4.3.7] Handbook of X-ray Photoelectron spectroscopy, (Perkin-Elmer Corporation, Physical Electronics Division, Minnesota, U.S.A., 1992)
[4.3.8] T. Ishida, H. Kobayashi and Y. Nakato, J. Appl. Phys, 73 (9), 4344 (1993)
[4.3.9] A.J. Nelson and H. Aharoni, J. Vac. Sci . Tech, A5 (2), 231 (1987)
[4.3.10] J.H. Thomas III and S.P. Sharma, J. Vac. Sci . Tech, 15 (5), 1707 (1978)
[4.3.11] A. Wakita, N. Moll and A. Fischer-Colbrie, J. Appl Phys, 68 (6), 2833 (1990)
[4.3.12] .R. Strohmeir, Surf. Interface Anal, 15, 51 (1990)
[4.3.13] I. Barin, in Thermochemical Data of Pure Substances (VCH Verlagsgesellschaft, Weinheim, Germany, 1989)
[4.3.14] R.S. Howell, S.K. Saha and M.K. Hatalis, "Cobalt and Nickel for Improved Aluminum-Indium Tin Oxide Contact Metallurgy in Polysilicon TFT Display Applications", Flat Panel Display Materials 1998 (MRS Symposium Proceedings, Vol 508) pp 321.

8 List of Publications of Work Accomplished

Under Government Funding

8.1 Journal Papers

1. "High performance thin film transistors in large grain size polysilicon deposited by thermal decomposition of disilane." *IEEE Transactions on Electron Devices,* Vol. 43, pp1399-1406, 1996. D. N. Kouvatsos, A. T. Voutsas, and M. K. Hatalis.
2. "Leakage current mechanism in submicron polysilicon thin film transistors." *IEEE Transactions on Electron Devices,* Vol 43, pp1218 - 1223, 1996. K. Olasupo and M. K. Hatalis.
3. "The effect of drain offset on current-voltage characteristics in sub-micron polysilicon thin film transistors." *IEEE Transactions Electron Devices,* Vol. 43, pp1306-1308, 1996. K. Olasupo, W. Yarbrough and M. K. Hatalis.
4. "Single crystal silicon thin film transistors fabricated at low process temperatures on glass substrates." *Electronics Letters*, Vol. 32, pp775 - 777, 1996. N. Kouvatsos, D. Tsoukalas, G. T. Sarcona, M. K. Hatalis and J. Stoemenos.
5. "Polycrystalline silicon thin film transistors fabricated at reduced thermal budgets by utilizing fluorinated gate oxidation." *IEEE Transactions on Electron Devices,* Vol. 43, pp1448 - 1453, 1996. D. N. Kouvatsos and M. K. Hatalis.
6. "Nickel Silicides Grown on Amorphous Silicon and Silicon-Germanium Thin Films." *Electrochemical and Solid State Letters*, Vol. 1, p233-234, 1998.
   G. Sarcona, S. K. Saha, and M. K. Hatalis
7. "Non-Erratic Behavior of Overerased Bits in Flash EEPROM." *Journal of Vacuum Science and Technology B*, vol. 16, p3065-3068, 1998. F. Nkansah, E. Prinz, and M. K. Hatalis
8. "Thin Film Transistors in Low Temperature As-deposited and Reduced Crystallization-Time Polysilicon on 665 C Strain Point Glass Substrates." *Thin Solid Films*, Vol. 338, pp281-285, (1999). M. K. Hatalis, D. N. Kouvatsos, J. H. Kung, A. T. Voutsas, and J. Kanicki
9. "Silicidation Reactions with Ci–Ni Bilayers for Low Thermal Budget Microelectronic Applications." *Thin Solid Films*, Vol. 347, pp278-283, (1999). S.K. Saha, R. S. Howell, and M. K. Hatalis
10. "Effect of Flash EEPROM Floating Gate Morphology on Electrical Behavior of Fast Programming Bits." *IEEE Transaction on Electron Devices,* Vol. 46, pp1355-1362. (1999). F. Nkansah and M. K. Hatalis
11. "Polysilicon Thin Film Transistors using Self-Aligned Cobalt and Nickel Silicide Source and Drain contacts." *IEEE Electron Device Letters,* Vol. 20, pp332-334 (1999). G. Sarcona, M. Stewart, and M. K. Hatalis.
12. "Elimination of Hillock Formation in Al Interconnects Using Ni or Co. "*Journal of Applied Physics,* Vol. 86, pp625-633, (1999). S. K. Saha, R. S. Howell, and M. K. Hatalis

13. "Reaction Mechanisms in Al-ITO Ohmic Contact Metallization with Co and Ni Barrier Layers for Active Matrix Display Applications." *Journal of Electrochemical Society,* Vol. 146, pp3134-3138, (1999). S. K. Saha, R. S. Howell, and M. K. Hatalis
14. "Polycrystalline Silicon Thin Film Transistors in Various Solid Phase Crystallized Films Deposited on Glass Substrates." *Journal of Electronic Materials*, Vol. 28, pp19-25 (1999). D. N. Kouvatsos, A. T. Voutsas, and M. K. Hatalis.
15. "Preparation and Stability of Low Temperature Cobalt and Nickel Silicides on Thin Polysilicon Films." *Journal of Vacuum Science and Technology A,* Vol. 18, pp97-93 (2000). R. S. Howell, G. Sarcona, and M. K. Hatalis.
16. "Poly-Si Thin Film Transistors on Steel Substrates." *IEEE Electron Device Letters,* Vol. 21, pp70-72 (2000). R. S. Howell, M. Stewart, S. V. Karnik, S. K. Saha, and M. K. Hatalis

8.2 Refereed Conference Proceedings Papers

1. "Low Temperature Silicides for Polysilicon Thin Film Transistor Applications." *Materials Research Society Symposium Proceedings,* vol. 402, pp191-196, 1996. G. Sarcona and M. K. Hatalis,
2. "Polysilicon Thin Film Transistors with Cobalt and Nickel Silicide Source and Drain Contacts." *Materials Research Society Symposium Proceedings,* vol. pp424. pp. 159-164, 1997. G. Sarcona and M. K. Hatalis.
3. "Helical Resonator Plasma Oxidation of Amorphous Silicon for Flat Panel Displays." *Materials Research Society Symposium Proceedings,* vol. 424. pp. 165-170, 1997. S. Kaluri, R. Howell, M. K. Hatalis and D. W. Hess.
4. "Polysilicon TFT Active Matrix Organic EL Displays." *SPIE Proceedings Series,* vol. 3057, pp.277-286, 1997. M. K. Hatalis, M. Stewart, C. Tang, and J. Burtis.
5. "Polysilicon Thin Film Transistors with Cobalt and Nickel Silicide Source and Drain Contacts." *Materials Research Society Symposium Proceedings,* vol. 424, pp. 159 - 164, 1997. G. Sarcona and M. K. Hatalis.
6. "Silicides for Polysilicon TFT-LCD applications." *SPIE Proceedings Series,* vol. 3014, pp141-146, 1997. R. S. Howell, M. J. Stewart, G. Sarcona, and M. K. Hatalis
7. "Polysilicon TFTs for AMLCD Applications with Gate Oxides Grown in a Low Temperature N2O Plasma." *SPIE Proceedings Series,* vol. 3014, pp170-175, 1997. R. S. Howell, S. R. Kaluri, M. K. Hatalis, and D. W. Hess
8. "Low Thermal Budget Polysilicon Crystallization by Rapid Thermal Processing." Proceedings of 1997 International Display Research Conference, ppL70-L73, 1997. H. Hovagimian, J. Mehlhaff, M. Stewart, M. Hatalis, and S. Saha.
9. "Polysilicon VGA Active Matrix OLED Displays: Technology and Performance." *IEEE Technical Digest of 1998 International Electron Device Meeting*, p871-874, 1998. M. Stewart, R. Howell, L. Pires, M. K. Hatalis, W. Howard, and O. Prache.
10. "Advanced Low Temperature Polysilicon TFT Technology for Active Matrix Flat Panel Displays." *SPIE Conference Proceedings*, vol. 3363, p278-287, 1998. M.K. Hatalis, M. Stewart, and R. Howell

11. "Low Temperature PECVD Polysilicon Crystallization by Rapid Thermal Processing." *Materials Research Society Symposium Proceedings*, vol. 508, p109-114, 1998. M. Stewart, H. Hovagimian, J. Arakkal, S. Saha, and M. K. Hatalis
12. "Cobalt and Nickel for Improved Aluminum-Indium Tin Oxide Contact Metallurgy in Polysilicon TFT Display Applications." *Materials Research Society Symposium Proceedings*, vol. 508, p321-326, 1998. R. S. Howell, S. K. Saha, and M. K. Hatalis
13. "Hillock Formation and Reduction Using metal Interlayers for Active Matrix Display Applications." *Materials Research Society Symposium Proceedings*, vol. 508, p333-338, 1998. S. K. Saha, R. S. Howell, and M. K. Hatalis.
14. "Advanced Polysilicon TFT Technology for Active Matrix Organic Light Emitting Diode Displays." *SPIE Conference Proceedings*, vol. 3363, p278-287, 1998.
15. "Preparation of Polycrystalline Silicon Thin Films by Rapid Thermal Crystallization and Applications." *The Electrochemical Society Proceedings of the 4th Symposium on Thin Film Transistor Technologies,* vol. 98-22, pp92-99, 1999. Miltiadis K. Hatalis, Mark Stewart and Howard Hovagimian.
16. "VGA Active Matrix OLED Displays Having the Single Polysilicon TFT Pixel Structure." *SPIE Conference Proceedings,* vol. 3636, pp22-31, 1999. M. K. Hatalis, M. Stewart, R. Howell, L. Pires, W. Howard, and O. Prache.
17. "Low Temperature Flat Panel Display Driver Circuits in RTP Crystallized Polysilicon." *Society for Information Display,* SID 99 Digest, pp. 460-463, 1999. M. Stewart, T. Afentakis, G. Sarcona, and M. K. Hatalis.

8.3 Other Conference Papers or Presentations

1. "Polysilicon TFT Active Layer Fabrication Processes." M. K. Hatalis. INVITED PAPER. Presented at the *"International Active Matrix Workshop"* held with the Euro Display '96: "The 16th International Display Research Conference." (October 1996). Paper published in the Proceedings of 1996 International Active Matrix Workshop, pp. 21-24, 1996.
2. "Preparation of Polycrystalline Silicon Thin Films by Rapid Thermal Crystallization and Applications. 1997 National Greek Conference on Solid State Physics. September 1997, Thessaloniki, Greece. Miltiadis K. Hatalis
3. "Thin film transistors fabricated at low thermal budgets in various types of polycrystalline silicon films on glass substrates", *Electrochemical Society Meeting Abstracts*, vol. 98-2, abstract No. 683, 1998. D. N. Kouvatsos, A. T. Voutsas and M. K. Hatalis.
4. "AMOLEDs with Rapid Thermal Processed (RTP) Polysilicon TFTs." *Proceedings of 1999 Vehicle Displays and Microsensors,* pp. 87-93, 1999. M. K. Hatalis, R. S. Howell, and M. Stewart.